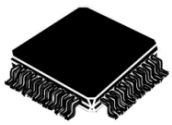
SPC1068

32-bit ARM Cortex-M3 based MCU with 14 channel PWMs, 16 channel 12-bit ADC, 3 PGAs with Comparators

Revision 14 – September 2021

Features

- ARM 32-bit Cortex-M3 CPU Core
  - Up to 150 MHz maximum frequency
- Memories
  - Up to 512 KB in-package flash
  - Up to 512 Bytes OTP flash
  - 48 KB on-chip SRAM
- Clock, reset and supply management
  - Single 3.3 V power supply
  - Power-On Reset (POR)
  - Brown-Out Detect (BOD)
  - 4 to 16 MHz external crystal oscillator
  - Two 24 MHz internal factory-trimmed RC oscillators
  - PLL for CPU clock
- 12-bit A/D converters (up to 16 channels)
  - As low as 125 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Dual-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Programmable gain amplifier (PGA)
  - Three integrated internal PGAs
  - Programmable Gains
    - Single-ended: 2, 4, 8, 16
    - Differential: 4, 8, 16, 32
  - Typical 600 ns settling time
- Analog comparator
  - Six high-speed comparators
  - Output with digital deglitch filter
  - Two DACs as reference
  - Out of range voltage protection



LQFP48 (7 x 7 mm)

- PWM
  - Seven enhanced PWM modules
  - 14 PWM outputs total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 34 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1 , SPI x 1, I^2C x 1
- Security Modules
  - CRC x 1, AES x 1
- Operating temperature
  - Junction temperature: -40 to +125 ^oC
  - Operating temperature: Industrial Class

Table 1. Ordering information

Ordering Number	In-package Flash	OTP Flash	Max CPU Frequency	Internal Crystal Oscillator	Package	Temperature Range	SPQ(1)	Packing
SPC1068BPE	512 KB	512 Bytes	150 MHz	Support	LQFP48	Industrial -40 °C ~ +125 °C	2500	Tray
SPC1068LBPE	128 KB (GigaDevice)	No OTP	100 MHz	Not support	LQFP48	Industrial -40 °C ~ +125 °C	2500	Tray

(1) SPQ = Standard Pack Quantity.

Table 2. In-package Flash feature differences between SPC1068 and SPC1068L

Items	SPC1068	SPC1068L
Flash Size	512 KB	128 KB
OTP Flash Size	512 Bytes	-
Page Program Time	0.7ms typical	0.4ms typical
Sector Erase Time (4KB)	30ms typical	45ms typical
Block Erase Time (32KB)	120ms typical	150ms typical
Block Erase Time (64KB)	150ms typical	250ms typical
Chip Erase Time	1s typical	3s typical

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1 Device overview

The SPC1068 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller. The SPC1068 incorporates a 32-bit ARM Cortex-M3 high-performance processor with a software-programmable clock rate as high as 150 MHz, 48 KB CODE/SRAM, in-package flash with 512 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 12-bit ADC, three PGAs, seven enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I^2C and a SPI. These features make the SPC1068 ideal for motor control application.

The SPC1068 operates from a 2.97 to 3.63 V power supply and is available in the -40 °C to +125 °C temperature range. The package type of SPC1068 is 48 pins.

Figure 1 shows the functional block diagram for the SPC1068. Figure 2 shows the clock tree information.

Figure 1. SPC1068 block diagram

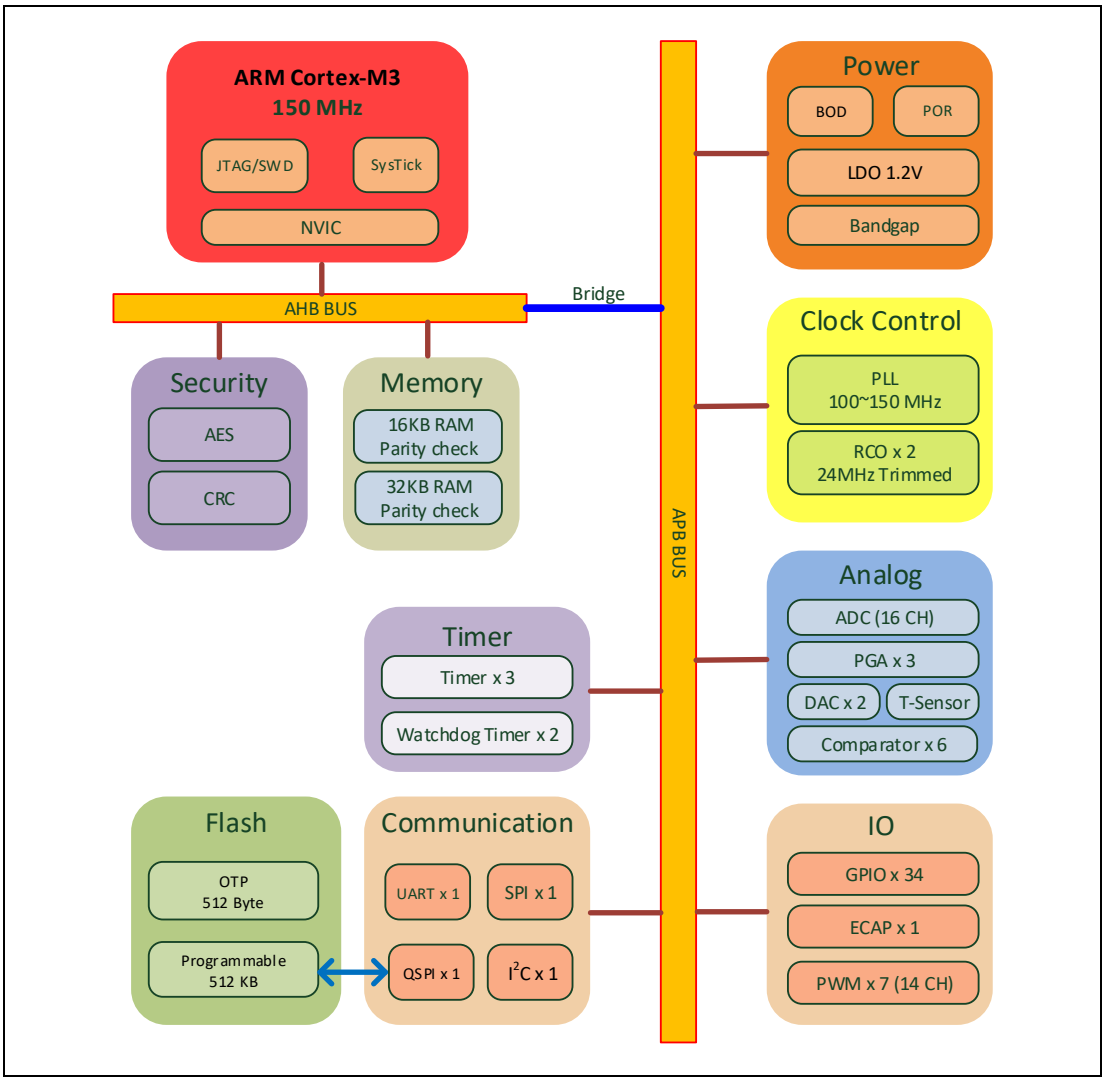
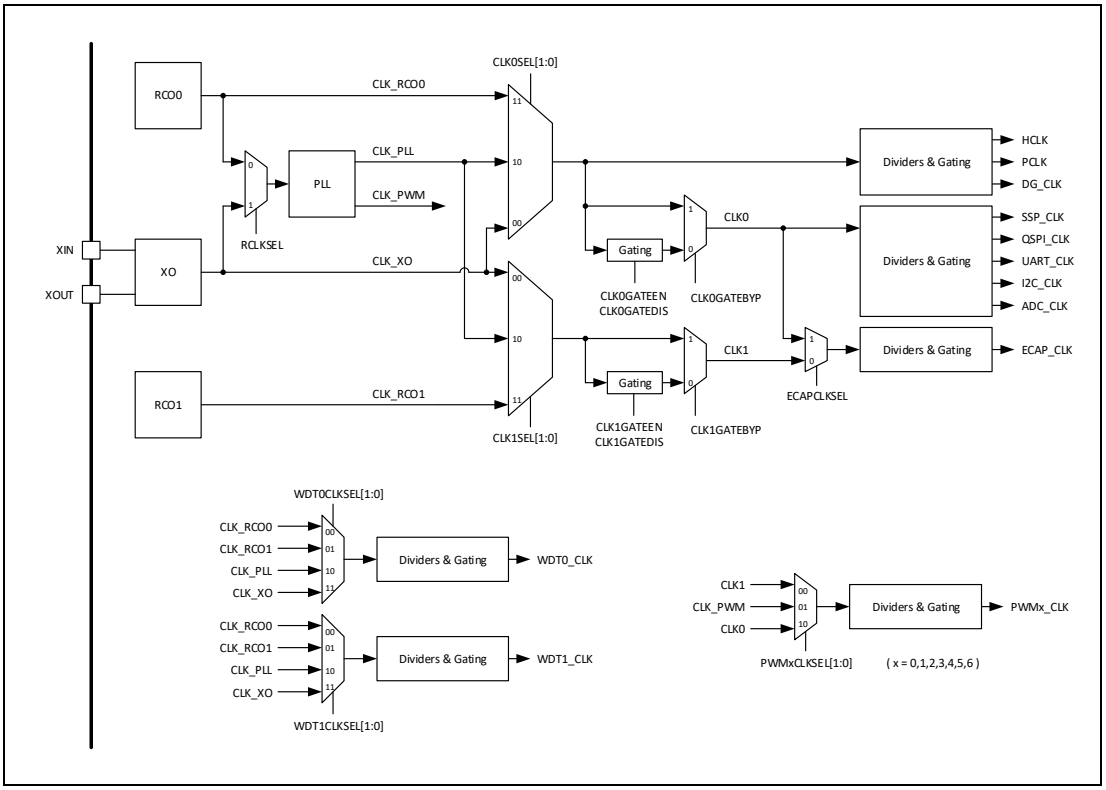


Figure 2. Clock tree



2 Feature descriptions

2.1 ARM Cortex-M3 core

The ARM Cortex-M3 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPC1068 integrates a full-feature ARM Cortex-M3 core. Therefore, it is compatible with all ARM tools and software. The processor can run up to 150MHz for SPC1068 and 100MHz for SPC1068L.

2.2 Embedded SRAM

The SPC1068 has implemented 48 KB of CODE/DATA SRAM memory. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 In-package Flash

The SPC1068 is integrated with in-package serial flash memory for storing programs and data, which is connected to QSPI interface. The features of the serial flash include:

- Total 512 KB flash memory for SPC1068 and 128 KB for SPC1068L
- 200 Mbps maximum serial data rate in Quad mode with 50 MHz operating clock
- Write protect all or portions of flash memory
- Sector erase (4KB) and Block erase (32 or 64 KB)
- Page program up to 256 bytes
- 512-byte OTP flash memory only for SPC1068

2.4 Nested vectored interrupt controller (NVIC)

The SPC1068 embeds a nested vectored interrupt controller able to handle up to 46 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPC1068 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply and Reset

The SPC1068 supports single power supply (3.3 V), which powers the IOs, internal voltage regulators and analog circuitry on chip. There are no special power-up sequencing requirements for the SPC1068.

The SPC1068 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.7 Brown-out detect

The device features an embedded brown-out detector (BOD) that monitors the V_{DD} power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when V_{DD} is higher or drops below the pre-set value. The interrupt service routine then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.8 Clocks

System clock selection is performed on startup, however the internal 24 MHz RC oscillator is selected as default CPU clock on reset. An external 4 - 16 MHz oscillator can be selected for SPC1068 and not for SPC1068L.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The PLL can provide 100 - 150 MHz clock for the core and PWM modules.

Several prescalers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency of the APB is 37.5 MHz. The peripherals frequency should not lower than APB bus frequency. See Figure 2 for details on the clock tree.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After a reset, the ARM processor begins code execution from this ROM. The boot pin is used to select one of the two boot options:

- Boot from in-package Flash (boot pin = 1): the boot loader copies user codes in the in-package flash to embedded SRAM, then runs code from SRAM
- ISP mode (boot pin = 0): the boot loader reprograms the in-package flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note: The boot pin can be configured as GPIO0. Be careful to use it in applications and can only be configured as output. Please make sure the pin level is high while the device is resetting or the device will enter ISP mode.

2.10 General-purpose IOs (GPIOs)

The SPC1068 can be configured to support as many as 34 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

Note 1: Boot pin can be configured as GPIO0.
Note 2: GPIO25 is test pin reserved for Spintrol.

2.11 Timers and watchdogs

The SPC1068 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPC1068 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. The clock of general-purpose timer is from APB clock (PCLK). However, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPC1068 implements two watchdogs. Each watchdog is based on a 32-bit down-counter. Each watchdog can be clocked from internal RC oscillator, external oscillator or PLL clock. Each watchdog can generate a reset or an interrupt when the counter reaches the given time-out value. Each watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.12 UART

The SPC1068 has an UART module that are functionally compatible with the 16550A and 16750 industry standards. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 7- or 8- bit characters
- Even, odd or no parity detection
- 1 stop-bit generation
- Baud-rate generation up to 3.6 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.13 I^2C

The I^2C bus interface complies with the common I^2C protocol and can operate in standard mode (with

data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 25 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

2.15 ADC

One 12-bit analog-to-digital convert is embedded into SPC1068 and has up to 16 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has two independent built-in sample-and-hold (S/H). Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 12-bit resolution
- 125 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Dual-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input short and disconnection detection for safety

Please see Table 10 for ADC characteristics.

2.16 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

2.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into SPC1068 and shares up to 16 channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains: Differential mode - 4, 8, 16, 32; Single-ended mode - 2, 4, 8, 16
- Settling time: 400 ns to 800 ns

Please see Table 11 for PGA characteristics.

2.18 Analog comparators

The SPC1068 has six high-speed comparators. Each comparator use the internal DAC as reference for monitoring PGA inputs or outputs. Two comparators are designed for each PGA: one is monitoring too-high voltage, the other is monitoring too-low voltage. The comparator output is routed to the PWM Trip Zone modules.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter

Please see Table 12 and Table 13 for analog comparator and DAC characteristics.

2.19 PWMs

The SPC1068 integrates seven PWM modules and supports 14 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.20 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPC1068 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter

- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.21 Cyclic redundancy check (CRC)

The SPC1068 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Four CRC standard polynomials supported

2.22 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

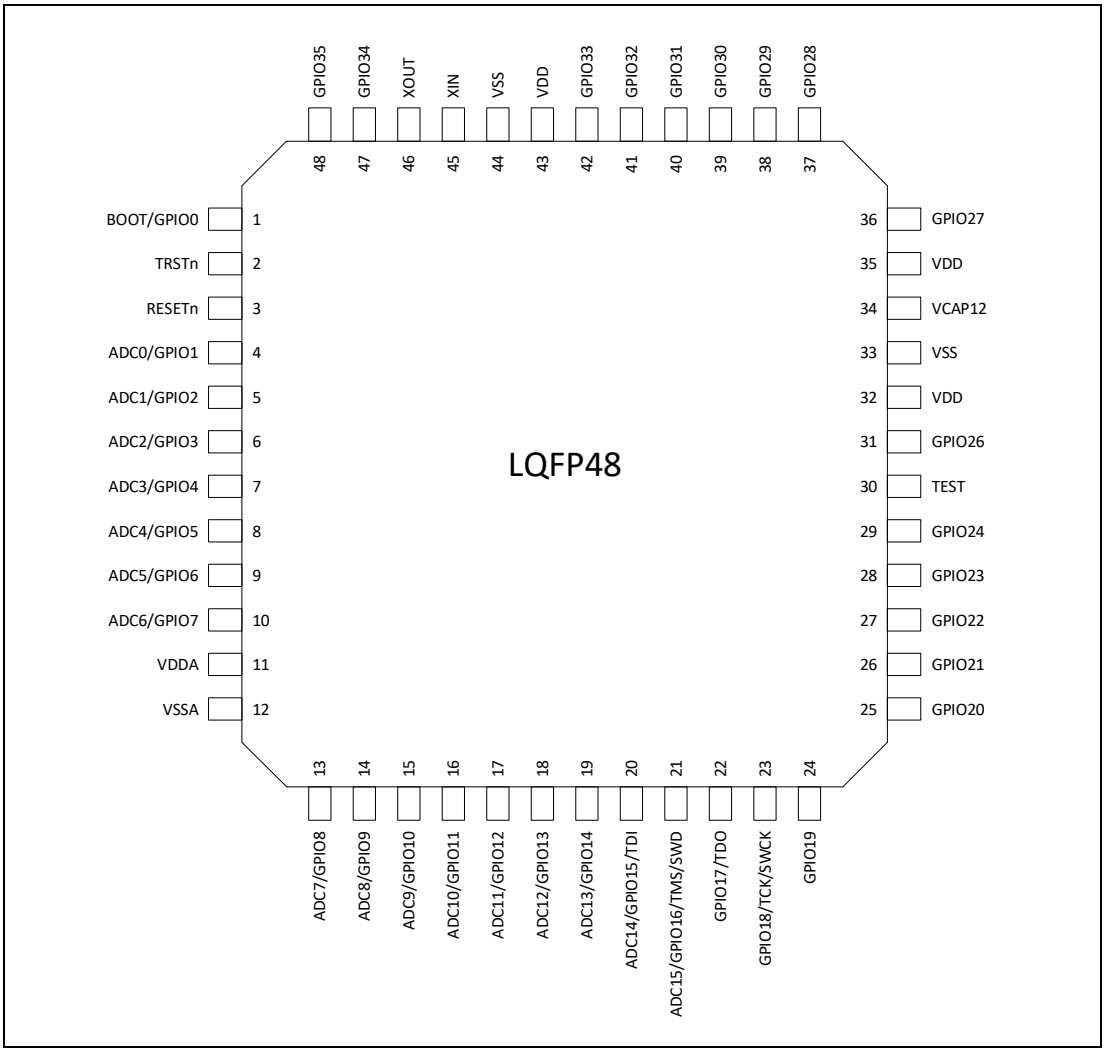
- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128-, 192-, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

2.23 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPC1068 certain security feature.

3 Pinouts and pin description

Figure 3. SPC1068 LQFP48 pinout



(1) The above figure shows the package top view.

(2) Note: when TRSTn is HIGH, GPIO15 ~ GPIO18 pins work as Debug interface and can't be configured as other functions.

Table 3. SPC1068 pin definitions

Pin	Signal	Type(1)	Description
1	BOOT(GPIO0)	I/O	Boot pin (General-purpose input/output 0)
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
2	TRSTn	I	JTAG reset pin, reset the JTAG when low
3	RESETn	I	Device reset pin, reset the device when low
4	ADC0	AI	ADC channel 0 input
	GPIO1	I/O	General-purpose input/output 1
	PWMSYNCI	I	External PWM synchronization pulse input
	PWMSYNCO	O	External PWM synchronization pulse output
	I2C_SDA	I/O	I^2C data

Table 3. SPC1068 pin definitions (continued)

Pin	Signal	Type[1]	Description
5	ADC1	AI	ADC channel 1 input
	GPIO2	I/O	General-purpose input/output 2
	PWM5B	O	PWM5 output B
6	ADC2	AI	ADC channel 2 input
	GPIO3	I/O	General-purpose input/output 3
	PWM5A	O	PWM5 output A
7	ADC3	AI	ADC channel 3 input
	GPIO4	I/O	General-purpose input/output 4
	PWM6B	O	PWM6 output B
8	ADC4	AI	ADC channel 4 input
	GPIO5	I/O	General-purpose input/output 5
	PWM6A	O	PWM6 output A
9	ADC5	AI	ADC channel 5 input
	GPIO6	I/O	General-purpose input/output 6
	PWM4B	O	PWM4 output B
10	ADC6	AI	ADC channel 6 input
	GPIO7	I/O	General-purpose input/output 7
	PWM4A	O	PWM4 output A
11	VDDA	S	Analog power pin
12	VSSA	S	Analog ground pin
13	ADC7	AI	ADC channel 7 input
	GPIO8	I/O	General-purpose input/output 8
	PWM4A	O	PWM4 output A
	COMP0HOUT	O	Output of comparator 0 of high-voltage
14	ADC8	AI	ADC channel 8 input
	GPIO9	I/O	General-purpose input/output 9
	PWM4B	O	PWM4 output B
	COMP1HOUT	O	Output of comparator 1 of high-voltage
15	ADC9	AI	ADC channel 9 input
	GPIO10	I/O	General-purpose input/output 10
	PWM6A	O	PWM6 output A
	COMP2HOUT	O	Output of comparator 2 of high-voltage
16	ADC10	AI	ADC channel 10 input
	GPIO11	I/O	General-purpose input/output 11
	PWM6B	O	PWM6 output B
	COMP0LOUT	O	Output of comparator 0 of low-voltage
17	ADC11	AI	ADC channel 11 input
	GPIO12	I/O	General-purpose input/output 12
	PWM5A	O	PWM5 output A
	COMP1LOUT	O	Output of comparator 1 of high-voltage

Table 3. SPC1068 pin definitions (continued)

Pin	Signal	Type[1]	Description
18	ADC12	AI	ADC channel 12 input
	GPIO13	I/O	General-purpose input/output 13
	PWM5B	O	PWM5 output B
	COMP2LOUT	O	Output of comparator 2 of high-voltage
19	ADC13	AI	ADC channel 13 input
	GPIO14	I/O	General-purpose input/output 14
20	ADC14	AI	ADC channel 14 input
	GPIO15	I/O	General-purpose input/output 15
	TDI	I	JTAG data input, **when TRSTn is HIGH, this pin always works as TDI**
21	ADC15	AI	ADC channel 15 input
	GPIO16	I/O	General-purpose input/output 16
	TMS/SWD	I/O	JTAG mode select or SWD data, **when TRSTn is HIGH, this pin always works as TMS/SWD**
22	GPIO17	I/O	General-purpose input/output 17
	TDO	O	JTAG data output, w**hen TRSTn is HIGH, this pin always works as TDO**
	TMS/SWD	I	JTAG mode select or SWD data
	SPI_FRM	I/O	SPI frame signal
	PWM6B	O	PWM6 output B
23	GPIO18	I/O	General-purpose input/output 18
	SPIMO	O	SPI master out
	TCK/SWCK	I	JTAG clock or SWD clock, **when TRSTn is HIGH, this pin always works as TCK/SWCK**
	I2C_SDA	I/O	I^2C data
	SPIMI	I	SPI master in
	PWM6A	O	PWM6 output A
24	GPIO19	I/O	General-purpose input/output 19
	SPICLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	CLK_TEST	O	Clock test pin
	I2C_SCL	I/O	I^2C clock
	SPICLK	I/O	SPI clock input/output
	PWM5B	O	PWM5 output B
25	GPIO20	I/O	General-purpose input/output 20
	SPI_FRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	PWM5A	O	PWM5 output A
26	GPIO21	I/O	General-purpose input/output 21
	SPIMI	I	SPI master in
	SPISO	O	SPI slave output
	PWM4B	O	PWM4 output B

Table 3. SPC1068 pin definitions (continued)

Pin	Signal	Type[1]	Description
27	GPIO22	I/O	General-purpose input/output 22
	SPIMO	O	SPI master out
	SPISI	I	SPI slave in
	PWM4A	O	PWM4 output A
28	GPIO23	I/O	General-purpose input/output 23
	PWM0B	O	PWM0 output B
	COMP0LOUT	O	Output of comparator 0 of low-voltage
29	GPIO24	I/O	General-purpose input/output 24
	PWM0A	O	PWM0 output A
	ATEST	I/O	Analog test pin
30	TEST	-	Test pin. Reserved for Spintrol.
31	GPIO26	I/O	General-purpose input/output 26
	I2C_SDA	I/O	I^2C data
	PWMSYNCI	I	External PWM synchronization pulse input
	ADCSOCAO	O	ADC start-of-conversion A
32	VDD	S	Digital power
33	VSS	S	Digital ground
34	VCAP12	S	1.2 V power
35	VDD	S	Digital power
36	GPIO27	I/O	General-purpose input/output 27
	I2C_SCL	I/O	I^2C clock
	PWMSYNCO	O	External PWM synchronization pulse output
	ADCSOCBO	O	ADC start-of-conversion B
37	GPIO28	I/O	General-purpose input/output 28
	PWM1A	O	PWM1 output A
	TDI	I	JTAG test data input
38	GPIO29	I/O	General-purpose input/output 29
	PWM1B	O	PWM1 output B
	COMP0HOUT	O	Output of comparator 0 of high-voltage
	TDO	O	JTAG test data output
39	GPIO30	I/O	General-purpose input/output 30
	PWM2A	O	PWM2 output A
	TMS/SWD	I/O	JTAG test-mode select or SWD data
40	GPIO31	I/O	General-purpose input/output 31
	PWM2B	O	PWM2 output B
	TCK/SWCK	I	JTAG test clock or SWD clock
41	GPIO32	I/O	General-purpose input/output 32
	PWM3A	O	PWM3 output A
	PWMSYNCI	I	External PWM synchronization pulse input
	PWMSYNCO	O	External PWM synchronization pulse output
	SPICLK	I/O	SPI clock input/output

Table 3. SPC1068 pin definitions (continued)

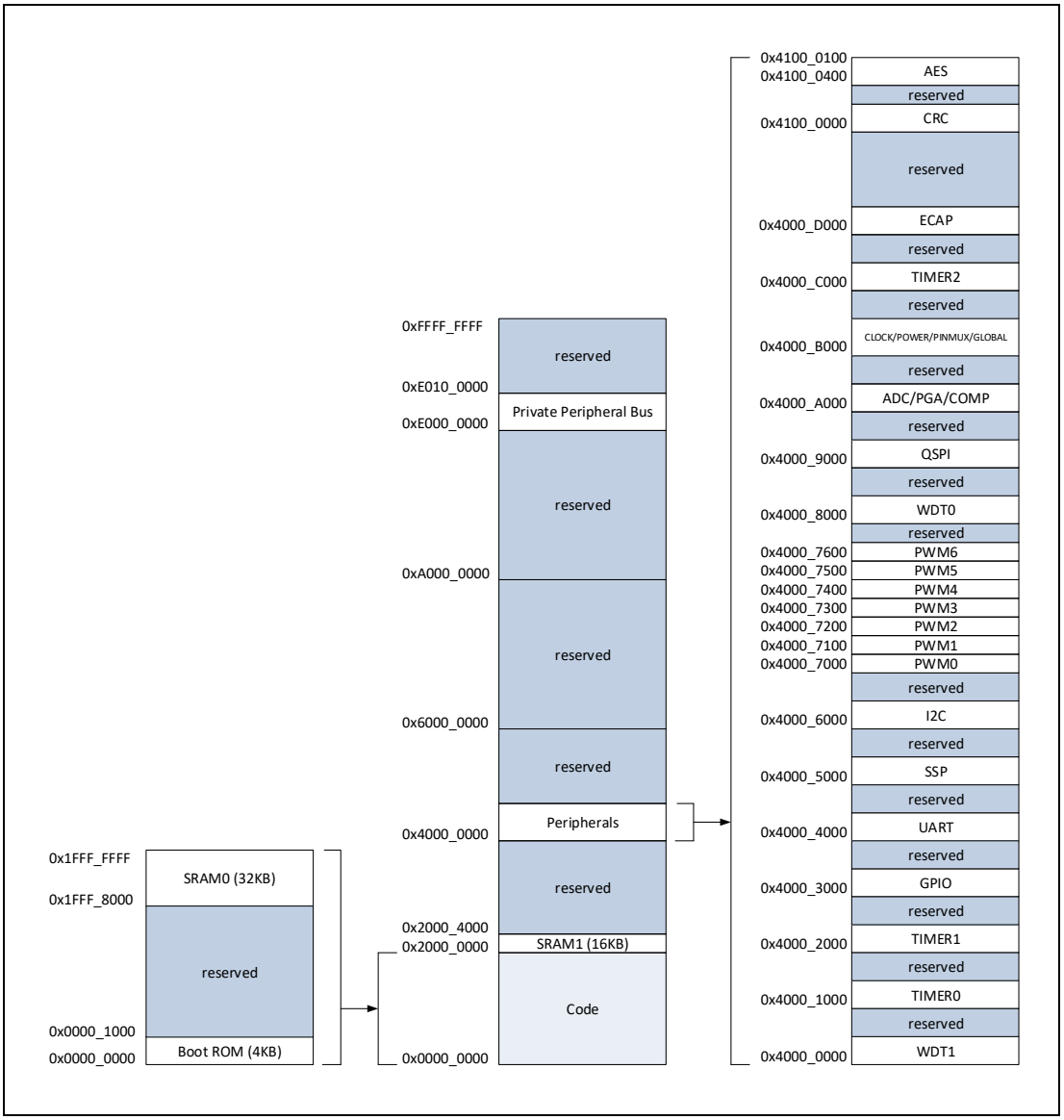
Pin	Signal	Type(1)	Description
42	GPIO33	I/O	General-purpose input/output 33
	PWM3B	O	PWM3 output B
	UART_RXD	I	UART receive data
	SPI_FRM	I/O	SPI frame signal
43	VDD	S	Digital power
44	VSS	S	Digital ground
45	XIN	AI	External oscillator input
46	XOUT	AO	External oscillator output
47	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
48	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	UART_TXD	O	UART transmit data

(1) I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

4 Memory mapping

The memory map of SPC1068 is shown in Figure 4.

Figure 4. Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 4. Absolute maximum ratings (1)(2)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_{stg}	Storage temperature(3)	-65	+150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	Supply voltage	-	2.97	3.3	3.63	V
V_{SS}	Supply ground	-	-	0	-	V
V_{DDA}	Analog supply voltage	-	2.97	3.3	3.63	V
V_{SSA}	Analog ground	-	-	0	-	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.4	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.6	V
I_{OH}	High-level output source current	V_{OH} = $V_{OH(MIN)}$	-	-	8	mA
I_{OL}	Low-level output sink current	V_{OL} = $V_{OL(MAX)}$	-	-	3.5	mA
T_J	Junction temperature	-	-40	-	+105	°C

5.3 Electrical characteristics

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	2.6	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
I_{IL}	Low-level input current (Pin with pull-up enabled)	V_{DD} = 3.3V, V_{IH} = 0 V	-	-	60	uA
I_{IH}	High-level input current (Pin with pull-up enabled)	V_{DD} = 3.3V, V_{IH} = V_{DD}	-	-	5	uA
I_{OZ}	Output current tri-state (Pin with pull-up disabled)	V_{DD} = 3.3V V_O = V_{DD}/0V	-	-	1	uA

5.4 Power consumption summary

Typical current consumption

In operational mode, the SPC1068 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module) are enabled;
- All peripheral clocks are as fast as HCLK, except ADC and QSPI;
- QSPI clock is configured as fast as PCLK;
- ADC clock setting: when $f_{HCLK} \leq 75$ MHz, $f_{ADC} = f_{HCLK}$; or else $f_{ADC} = f_{HCLK}/2$;
- All clock modules are enabled;
- Select PLL clock as system clock source.

In idle mode, the SPC1068 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module) are clocked off or disabled;
- Clock modules(PLL, RCO1 and XO) are disabled;
- Select RCO0 as system clock source.

The SPC1068 device typical current consumption is shown in Table 7 and Figure 5 shows the operational current consumption versus HCLK frequency.

Table 7. SPC1068 typical current consumption

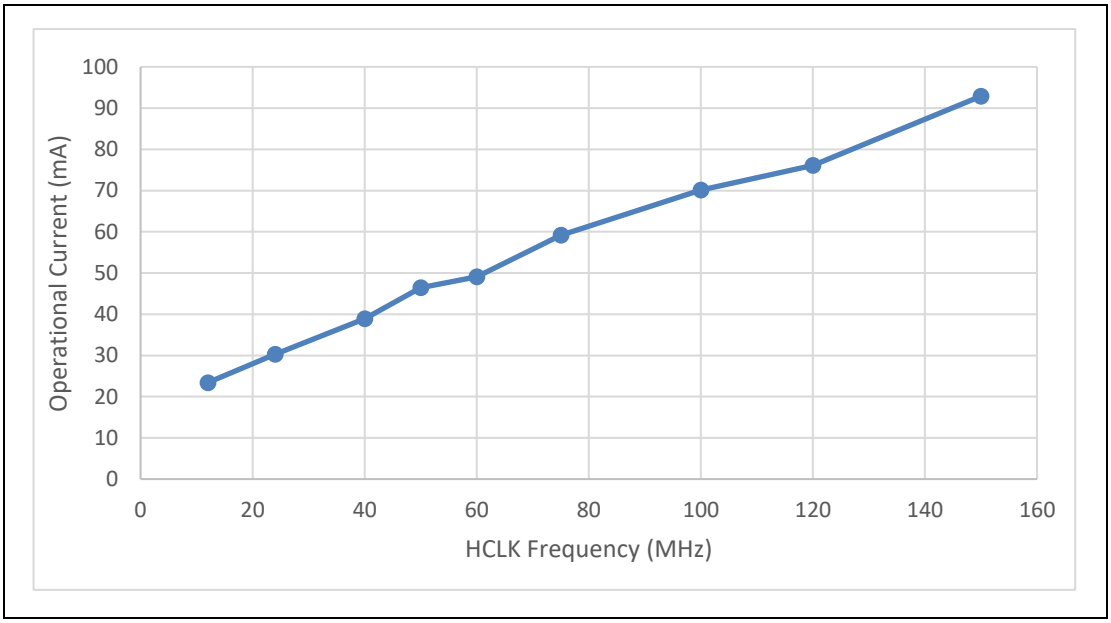
Mode	Conditions			Typ[2]	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
Operational[1]	150 MHz[3]	37.5 MHz	150 MHz	92.9	mA
	120 MHz[3]	30 MHz	120 MHz	76.1	mA
	100 MHz	25 MHz	100 MHz	70.1	mA
	75 MHz	37.5 MHz	150 MHz	59.2	mA
	60 MHz	30 MHz	120 MHz	49.1	mA
	50 MHz	37.5 MHz	150 MHz	46.4	mA
	40 MHz	30 MHz	120 MHz	38.9	mA
	24 MHz	24 MHz	120 MHz	30.3	mA
	12 MHz	12 MHz	120 MHz	23.4	mA
Idle	400 kHz	400 kHz	-	1.79	mA

(1) If the SPC1068 reads, programs or erase its flash, additional current will be consumed (typically, 7 mA for reading and 20 mA for programming or erasing).

(2) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

(3) The maximum HCLK frequency of SPC1068L is 100MHz. Functionality for frequency above 100MHz is not guaranteed.

Figure 5. Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 8. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO1 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

Table 8. Peripheral current consumption

Peripherals[1]	Conditions	Typ[2]	Unit
BOD	Select RCO0 as system clock source; All other peripherals are in default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	0.10	mA
Bandgap[2]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK except QSPI; f_{HCLK} = 60 MHz, f_{PCLK} = 30 MHz, f_{QSPI} = 30 MHz f_{PLL} = 120 MHz	44.2	uA
ADC (Analog Part)		4.49	mA
T-Sensor		33.7	uA
PGA[3]		145.2	uA
DAC		7.8	uA
Comparator		38.7	uA
ADC (Digital Part)		2.72	mA
UART		0.42	mA
I2C		0.74	mA
SPI		0.76	mA
QSPI		0.21	mA
PWM		1.45	mA
ECAP		0.55	mA
WDT		0.09	mA
XO[4]		2.16	mA
RCO		0.77	mA
PLL	Select RCO0 as system clock source; All other peripherals are in default settings; f_{PLL} = 120 MHz	1.50	mA

(1) For peripherals with multiple instances, the current quoted is for per module. For example, the 1.45 mA value quoted for PWM is for one PWM module.

(2) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

(3) The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

(4) XO is not supported in SPC1068L.

5.5 Internal regulator characteristics

Table 9. Internal regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
VCAP12	Output voltage	Light load[1]	1.14	1.2	1.26	V
		Heavy load[2]	1.14	1.2	1.26	V

(1) Light load case = Chip starts up as default.

(2) Heavy load case = Set PLL frequency to 150 MHZ, turn on all PWM modules

5.6 12-bit ADC characteristics

Table 10. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	12	-	-	bit
F_S	Conversion speed	-	-	-	4	MSPS
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{REF}	Reference voltage	-	1.19	1.2	1.21	V
I_{PAD}	Operational current	V_{DDA} = 3.3 V	-	5.8	6.96	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{OFF}	Offset error	Without calibration	-60	-	60	LSB
E_{GAIN}	Gain error	Without calibration	-120	-	120	LSB
E_{OFF2}	Channel to channel offset	-	-4	-	4	LSB
E_{GAIN2}	Channel to channel gain error	-	-30	-	30	LSB
T_{COEF}	ADC temperature coefficient with internal reference	-	-	30	-	ppm/°C
t_{PWRUP}	Power-up time	-	-	-	200	us
SNR	Signal-to-noise ratio	Fin = 10 kHz, Amp = 0.94F_S, N = 8192	-	65.0	-	dB
THD	Total harmonic distortion		-	76.6	-	dB
ENOB	Effective number of bits		-	10.5	-	bit
SFDR	Spurious free dynamic range		-	79.6	-	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	-	-	3.8473	-	°C/LSB
T_{OFFSET}	ADC output at 50 °C of the temperature sensor	-	-	4182	-	LSB

5.7 PGA characteristics

Table 11. PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage range	-	0.4	-	V_{DDA}-0.4	V
R_{IN}	Input impedance	-	-	Hi-Z	-	Ω
G	Gain	Single-ended mode	2, 4, 8, 16			-
		Differential mode	4, 8, 16, 32			-
E_{GAIN}	Gain error	G = 2, Single-ended mode	-1.50	-	1.50	%
		G = 16, Single-ended mode	-4.00	-	4.00	%
V_{OS}	Offset	-	-15	-	15	mV
t_{SETTLE}	Settle time	G = 2, Single-ended mode	-	-	388	ns
		G = 16, Single-ended mode	-	-	500	ns
I	Current consumption	Only one PGA	-	400	700	uA

5.8 Analog comparator characteristics

Table 12. Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage	-	-15	-	15	mV
V_{HYST}	Hysteresis voltage	-	-60	-	60	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	-	-	40	-	ns

5.9 Internal DAC characteristics

Table 13. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_{CM}	Current mode resolution	Monotonic, no missing code	10	-	-	bit
V_{FS}	Full scale value	Operating in current mode with double range option	1.84	-	2.70	V
DNL	Differential linearity	-	-1	-	1	LSB
INL	Integral linearity	-	-3	-	3	LSB
E_{OFF}	Offset error	-	-50	-	50	mV
N_{VM}	Voltage mode resolution	Monotonic, no missing code	7	-	-	bit
t_{SETTLE}	DAC settling time	Design guarantee	-	10	-	us

5.10 Flash memory characteristics

The characteristics are given at T_J = -40 to 105 °C unless otherwise specified.

Table 14. Flash memory characteristics (SPC1068)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BP1}	Byte program time (first byte)(1)	Winbond	-	15	30	us
		GigaDevice	-	40	70	us
t_{BP2}	Additional byte program time (after first byte)(1)	Winbond	-	2.5	5	us
		GigaDevice	-	2.5	12	us
t_{PP}	Page program time	Winbond	-	0.4	0.8	ms
		GigaDevice	-	0.4	2	ms
t_{SE}	Sector erase time (4KB)	Winbond	-	30	300	ms
		GigaDevice	-	45	300	ms
t_{BE1}	Block erase time (32KB)	Winbond	-	120	800	ms
		GigaDevice	-	150	1200	ms
t_{BE2}	Block erase time (64KB)	Winbond	-	150	1000	ms
		GigaDevice	-	250	1600	ms
t_{CE}	Chip erase time	Winbond	-	1	4	s
		GigaDevice	-	3	10	s
N_{END}	Endurance (erase/write cycle)	-	100k	-	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	20	-	-	years

(1) For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

Table 15. Flash memory characteristics (SPC1068L)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BP1}	Byte program time (first byte)(1)	-	-	30	50	us
t_{BP2}	Additional byte program time (after first byte)(1)	-	-	2.5	12	us
t_{PP}	Page program time	-	-	0.6	2.4	ms
t_{SE}	Sector erase time (4KB)	-	-	45	300	ms
t_{BE1}	Block erase time (32KB)	-	-	150	700	ms
t_{BE2}	Block erase time (64KB)	-	-	250	800	ms
t_{CE}	Chip erase time	-	-	2.5	6.5	s
N_{END}	Endurance (erase/write cycle)	-	100k	-	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	20	-	-	years

(1) For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

5.11 Electrical sensitivity characteristics

Table 16. ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	-	500	V
			Corner Pin	750	V

Table 17. Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{DD} = 3.63V, VCAP12 = 1.32V	100	mA

5.12 Moisture sensitivity characteristics

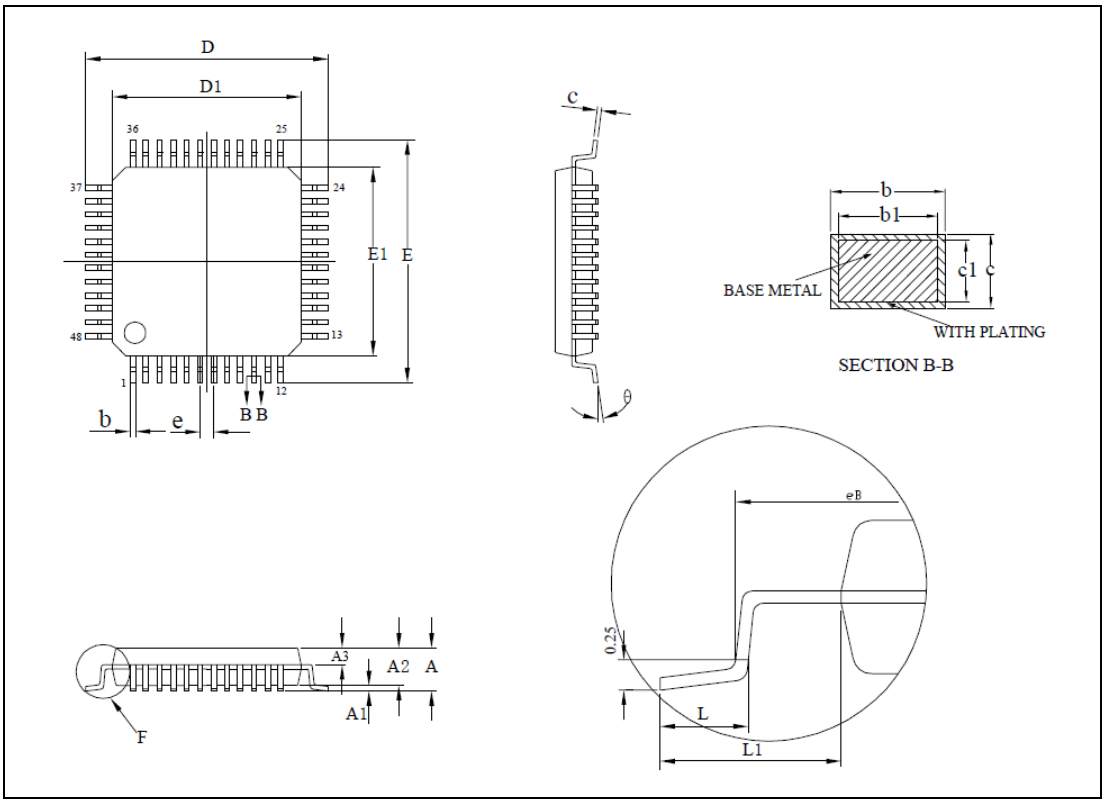
Table 18. Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	-	Level 3	-

6 Package information

The package type of SPC1068 is 48-pin low-profile quad flat package (LQFP48). The detail information is as follows:

Figure 6. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package outline



(1) Drawing is not to scale.

Table 19. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data

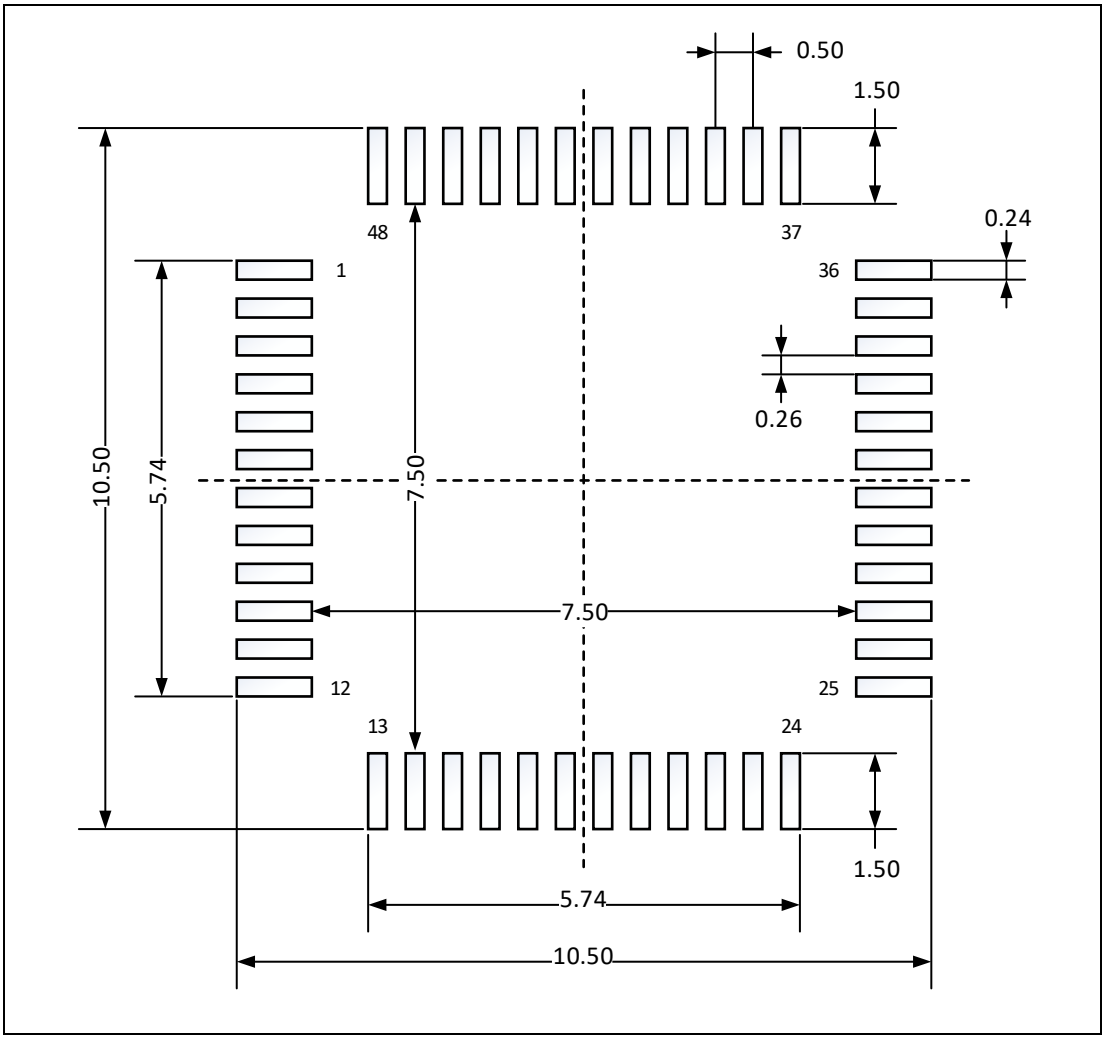
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
A3	0.59	0.64	0.69	0.0232	0.0252	0.0272
b	0.18	-	0.26	0.0071	-	0.0102
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	-	0.17	0.0051	-	0.0067
c1	0.12	0.13	0.14	0.0047	0.0051	0.0055
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
eB	8.10	-	8.25	0.3189	-	0.3248

Table 19. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.5	-	-	0.0197	-
L	0.45	-	0.75	0.0177	-	0.0295
L1	-	1.00	-	-	0.0394	-
θ	0	-	7°	0	-	7°

(1) Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 7. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package recommended footprint



(1) Dimensions are expressed in millimeters.

7 Revision history

Table 20. Document revision history

Date	Revision	Changes
11-Jan-2017	1	Initial release.
3-May-2017	2	1. Updates VOH, VOL, IOH, IOL parameter values in Table 5. Recommended operating conditions. 2. Updates all parameter values in Table 6. Electrical characteristics.
4-July-2017	3	1. Modifies Figure 2. Clock tree.
25-Jan-2018	4	1. Updates SPC1068 package type to LQFP48. 2. Modifies A1, L parameter values in Table 19. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data.
20-Nov-2018	5	1. Add Table 1. Ordering information.
20-Dec-2018	6	1. Modifies Table 4. Absolute maximum ratings (1)(2). 2. Modifies Table 5. Recommended operating conditions.
15-Jan-2019	7	1. Modifies Table 1. Ordering information.
20-Mar-2019	8	1. Add Table 14. Flash memory characteristics.
5-May-2019	9	1. Highlight SPC1068L maximum frequency difference in Section 2.1 and Table 7. SPC1068 typical current consumption. 2. Highlight SPC1068L Flash size difference in Section 2.3. 3. Highlight XO is not supported in SPC1068L in Section 2.8 and Table 8. Peripheral current consumption.
28-Jun-2019	10	1. Modifies Table 1. Ordering information.
15-Aug-2019	11	1. Modifies JTAG and RESETn pin descriptions in Table 3. SPC1068 pin definitions.
20-Dec-2019	12	1. Add Table 16. ESD absolute maximum ratings. 2. Add Table 17. Electrical sensitivities.
15-Jan-2020	13	1. Modifies ADC (Analog part) current consumption in Table 8. Peripheral current consumption.
27-Sep-2021	14	1. Update Table 1. Ordering information for SPC1068 information. 2. Add Table 2. In-package Flash feature differences between SPC1068 and SPC1068L. 3. Update Figure 3. SPC1068 LQFP48 pinout. 4. Update Table 14. Flash memory characteristics (SPC1068) for GigaDevice flash. 5. Add Table 15. Flash memory characteristics (SPC1068L). 6. Add Table 18. Moisture sensitivity characteristic. 7. Modifies b, b1, c, L parameter values in Table 19. LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data.