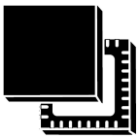
SPD1148

32-bit MCU with 14-bit ADC, 3 PGAs with Comparators, Buck DC/DC and LDO, integrated 3-phase Pre-Driver with supply up to 42V

Revision 11 – September 2022

Features

- 32-bit ARM Cortex-M4 CPU Core with FPU
  - 200MHz maximum frequency
- Memories
  - Up to 128 KB embedded flash
  - 512 Bytes OTP flash
  - Up to 64 KB on-chip SRAM
- Power Management
  - Integrated Buck DC-DC for MCU and main I/O supply
  - Integrated LDO for pre-driver supply
- Pre-Driver Module
  - 3-Phase Pre-Driver for BLDC motor control application with 42V max input voltage and down to 5.5V input voltage functionality
  - Integrated bootstrap diodes
  - Integrated charge pump for 100% duty cycle
  - 1A pull-up and 1.3A pull-down option
  - Programmable output swing from 8V to 18V
  - Six external power FET V_{DS} monitors
- Clock, reset and supply management
  - Brown-out Detect (BOD) on each power rail
  - Power-On Reset (POR)
  - 1 to 66 MHz external crystal oscillator
  - Internal 32 MHz factory-trimmed oscillator
  - Internal 2.2MHz backup-safety clock
  - PLL for CPU clock
- 14-bit A/D converters (up to 9 channels)
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor



QFN48 (7 x 7 mm, 0.5mm pitch)
QFN60 (9 x 9 mm, 0.5mm pitch)

- Programmable gain amplifier (PGA)
  - Three integrated internal PGAs
  - Programmable Gains
    - Single-ended: 1,2,4,8,12,16,24,32
    - Differential: 2,4,8,16,24,32,48,64
  - Typical 600 ns settling time
- Analog comparator
  - Ten high-speed comparators
  - Output with digital deglitch filter
  - 4 DACs as reference
  - Optional DAC output buffer
  - Out of range voltage protection
  - Phase comparison
- PWM
  - Internal PWM signals to embedded Pre-Driver
  - Signal generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 31 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and PWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces

- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1, SPI x 1, I^2C x 1, SIO x 1
  - SIO can be configured as CAN, SPI, UART, I2C, etc.
- Deep sleep mode with off current as low as 6uA and pin wake-up
- Security modules
  - CRC x 1, AES x 1, 64-bit unique ID
- Operating temperature
  - Junction temperature: -40 to +125 °C
  - Ambient temperature: -40 to +105 °C

Contents

1 Device overview 7

2 Feature descriptions 11

2.1 ARM Cortex-M4 core 11
2.2 Embedded SRAM 11
2.3 Embedded Flash memory 11
2.4 Nested vectored interrupt controller (NVIC) 11
2.5 External interrupt/event controller 11
2.6 Power supply, reset and deep sleep mode 11
2.7 Brown-out detector 12
2.8 Clocks 12
2.9 Boot mode 12
2.10 General-purpose Ios (GPIOs) 13
2.11 Timers and watchdogs 13
2.12 UART 13
2.13 I^2C 14
2.14 SPI 14
2.15 ADC 14
2.16 Temperature sensor 15
2.17 PGAs 15
2.18 Analog comparators 15
2.19 PWMs 15
2.20 ECAP 16
2.21 Cyclic redundancy check (CRC) 16
2.22 Advanced encryption standard (AES) engine 16
2.23 Serial wire JTAG debug port (SWJ-DP) 16
2.24 SIO 16
2.25 Power management module 17
2.26 Pre-Driver system 17

3 Pinout and pin description 18

3.1 QFN48 18
3.2 QFN60 23
3.3 PGA input channel selection 29
3.4 GPIO pin function and state after reset 29

4 Memory mapping 31

5 Electrical characteristics 32

5.1 Absolute maximum ratings 32
5.2 Recommended operating conditions 33
5.3 I/O Electrical characteristics 34
5.4 Power consumption summary 34
5.5 Internal 1.2V regulator characteristics 39
5.6 BOD characteristics 40
5.7 RCO characteristics 40
5.8 PLL characteristics 40
5.9 XO characteristics 40
5.10 14-bit ADC characteristics 45
5.11 PGA characteristics 46
5.12 Analog comparator characteristics 47
5.13 Internal 10-bit DAC characteristics 47
5.14 DAC buffer characteristics 47
5.15 Flash memory characteristics 48
5.16 Electrical sensitivity characteristics 48
5.17 Moisture sensitivity characteristics 49
5.18 Thermal resistance characteristics 49
5.19 SPI characteristics 49
5.20 Pre-Driver characteristics 50
5.21 VDDG LDO characteristics 57
5.22 Buck DC-DC regulator characteristics 58

6 PCB layout guidance 62

7 Package information 64

7.1 QFN48 64
7.2 QFN60 66

8 Ordering information 67

9 Revision history 68

List of tables

Table 1. SPD1148 QFN48 pin definitions 18
Table 2. SPD1148 QFN60 pin definitions 23
Table 3. PGA input channel selection 29
Table 4. GPIO pin function and state after reset 29
Table 5. Absolute maximum ratings (1)(2) 32
Table 6. Recommended operating conditions 33
Table 7. I/O Electrical characteristics 34
Table 8. SPD1148 typical current consumption (Run in FLASH) 35
Table 9. SPD1148 typical current consumption (Run in RAM) 36
Table 10. Peripheral current consumption 37
Table 11. Internal 1.2V regulator characteristics 39
Table 12. BOD characteristics 40
Table 13. RCO characteristics 40
Table 14. PLL characteristics 40
Table 15. XO characteristics 40
Table 16. ADC characteristics 45
Table 17. PGA characteristics 46
Table 18. Comparator characteristics 47
Table 19. DAC characteristics 47
Table 20. DAC buffer characteristics 47
Table 21. Flash memory characteristics 48
Table 22. ESD absolute maximum ratings 48
Table 23. Electrical sensitivities 48
Table 24. Moisture sensitivity characteristic 49
Table 25. Thermal resistance characteristics (QFN48 package) 49
Table 26. SPI characteristics 49
Table 27. Pre-Driver characteristics 50
Table 28. Internal VDDG regulator characteristics 57
Table 29. Buck DC-DC regulator characteristics 58
Table 30. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead package mechanical data 64
Table 31. QFN60 – 60 pin, 9mm x 9mm quad flat no-lead package mechanical data 66
Table 32. Ordering information 67
Table 33. Document revision history 68

List of figures

Figure 1. SPD1148 functional block diagram 8
Figure 2. Clock tree 9
Figure 3. Typical application diagram 10
Figure 4. SPD1148 QFN48 pin-out 18
Figure 5. SPD1148 QFN60 pin-out 23
Figure 6. Memory map 31
Figure 7. Typical operational current versus frequency 36
Figure 8. Deep sleep mode leakage vs. VBAT level 38
Figure 9. Internal 1.2V regulator load regulation (T_A = 25 °C) 39
Figure 10. Internal 1.2V regulator load regulation with different temperature 39
Figure 11. The negative resistance of the on-chip crystal oscillator at 50℃ 41
Figure 12. The negative resistance of the on-chip crystal oscillator at 85℃ 42
Figure 13. The negative resistance of the on-chip crystal oscillator at 100℃ 43
Figure 14. The negative resistance of the on-chip crystal oscillator at 125℃ 44
Figure 15. DAC buffer offset over Input voltage 48
Figure 16. Pre-Driver maximum sourcing current measurement 51
Figure 17. Pre-Driver maximum sinking current measurement 51
Figure 18. Pre-Driver toggling at VBAT=44V 52
Figure 19. Pre-Driver toggling at VBAT=5V 52
Figure 20. Low-side propagation delay measurements (rising edge) 53
Figure 21. Low-side propagation delay measurements (falling edge) 53
Figure 22. High-side propagation delay measurements (rising edge) 54
Figure 23. High-side propagation delay measurements (falling edge) 54
Figure 24. Demonstration of -10V support for all phases toggling in-phase 55
Figure 25. Pre-Driver system response during VBAT power step (from 17V to 40V) 55
Figure 26. Pre-Driver system response during VBAT power step (from 40V to 17V) 56
Figure 27. VDDG LDO load regulation for 10V programmable option 57
Figure 28. Buck efficiency for different levels of input power VBAT and current loads 58
Figure 29. Buck load regulation 59
Figure 30. Buck load regulation and current capability for low VBAT levels 59
Figure 31. Response of DVDD to VBAT step (from 17V to 40V) 60
Figure 32. Response of DVDD to VBAT step (from 40V to 17V) 60
Figure 33. Buck output response to current step at VBAT=24V (from 23mA to 500mA) 61
Figure 34. Buck output response to current step at VBAT=24V (from 500mA to 23mA) 61
Figure 35. Simplified Pre-Driver Board Diagram 63
Figure 36. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead package outline 64
Figure 37. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead recommended footprint 65
Figure 38. QFN60 – 60 pin, 9mm x 9mm quad flat no-lead package outline 66

1 Device overview

SPD1148 is a SiP (System in a Package) device integrating MCU, Pre-Driver module and power management module to have “all-in-one” chip for BLDC motor driving application with supply voltage up to 42V.

The MCU incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 200 MHz, 64 KB SRAM, embedded flash with 128 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 14-bit ADC, three PGAs, six enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I^2C and a SPI. These features make the SPD1148 ideal for motor control application.

The Pre-Driver module provides three half-bridge pre-drivers, with programmable charging /discharging current capability up to 1A. Integrated Charge Pump supports 100% duty cycle.

The Power management module includes a 42V maximum input, 3.3V 300mA output buck DC-DC regulator, and Brown-out-Detection observing each of the power rail.

The temperature range is from -40 °C to +125 °C. The package type is 48-pin or 60-pin QFN.

Figure 1 shows the functional block diagram for the SPD1148. Figure 2 shows the clock tree information. Figure 3 shows the typical application diagram.

Figure 1. SPD1148 functional block diagram

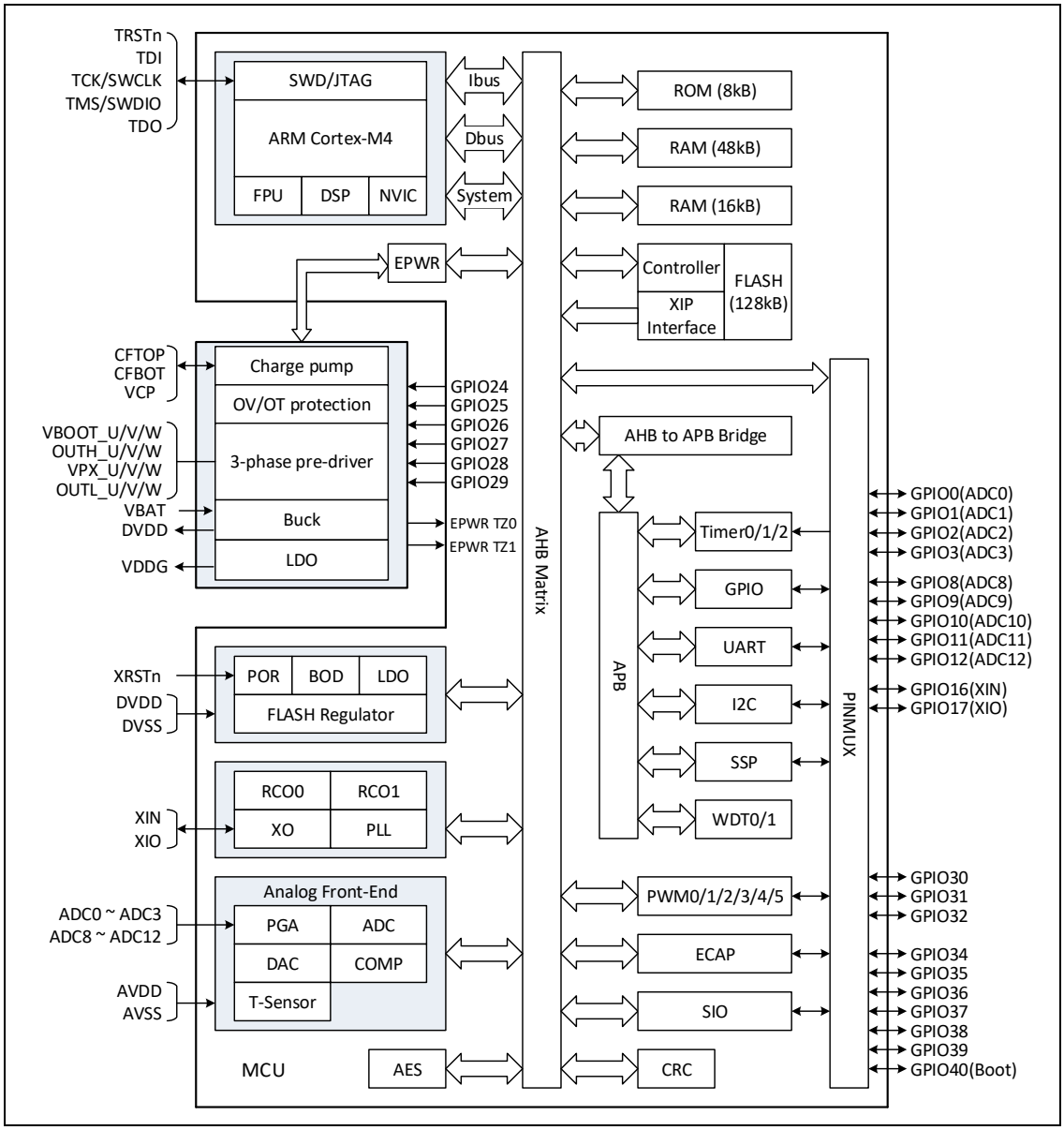


Figure 2. Clock tree

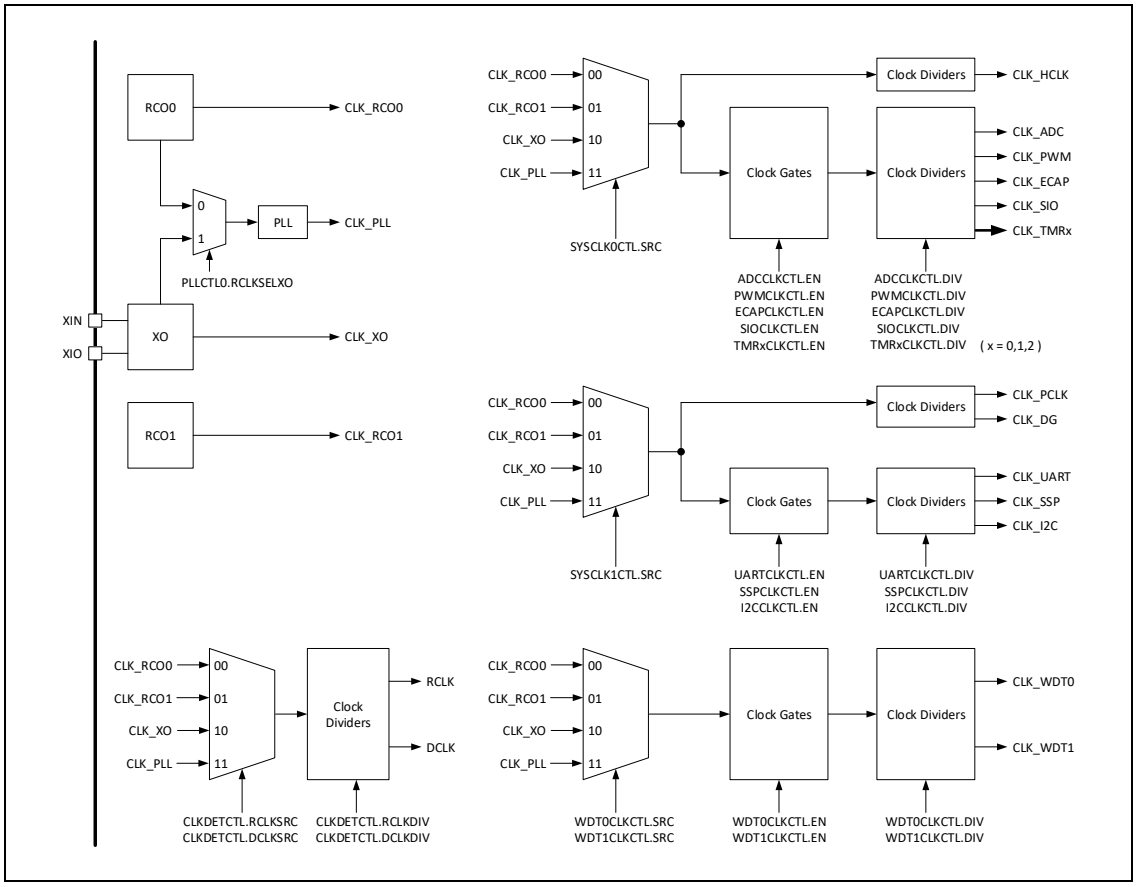
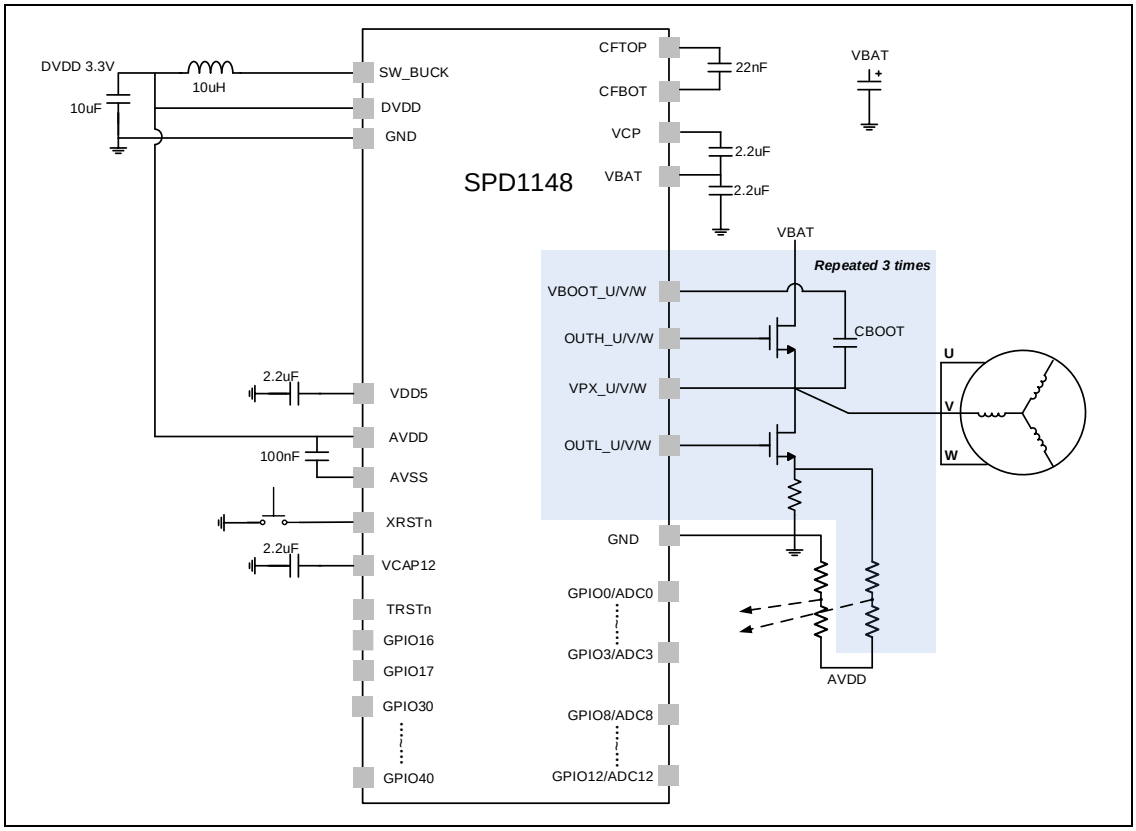


Figure 3. Typical application diagram



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1148 integrates a full-feature ARM Cortex-M4 core with FPU that can run up to 200MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Embedded SRAM

The SPD1148 has implemented 64 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data.

2.4 Nested vectored interrupt controller (NVIC)

The SPD1148 embeds a nested vectored interrupt controller able to handle up to 51 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPD1148 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply, reset and deep sleep mode

The SPD1148 requires a single 5.5V to 42V power supply. All derivative supplies such as low-side pre-driver supply, main digital MCU 3.3V supply, MCU 1.2V supply are generated on-chip from a single input supply. External generation option for derivative supplies is also available.

The SPD1148 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

Deep sleep mode option is provided, during which the Buck DC-DC will be disabled and all the control blocks are disabled except reset monitoring logic which is used to wait for wake-up command. The only functioning internal power will be VDD5. During deep sleep mode the total chip current can be as low as 6uA. To wake up from the deep sleep mode reset pin has to be toggled.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the main input supply VBAT, low-side pre-driver supply VDDG, main digital MCU 3.3V supply V_{DD} and MCU 1.2V supply voltage levels and compare them to the programmable pre-set values. An interrupt or reset can be generated when voltage of any of the power domains is higher or lower their respective pre-set values. The interrupt service routine will then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software. The MCU BOD for 3.3/1.2V supplies is implemented inside the MCU, separately from high-voltage BOD system.

2.8 Clocks

The MCU system clock selection is performed on startup. The internal 32 MHz RC oscillator is selected by default upon reset. An external 1 – 66 MHz oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The output frequency covers range from 25MHz to 200MHz.

Several clock dividers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency is 200MHz for AHB and 50 MHz for APB. See Figure 2 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 2.2MHz backup-safety oscillator makes the SPD1148 get rid of clock stuck.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (boot pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note 1: The boot pin should always keep high when chip normally running.

Note 2: The TRSTn pin is recommended to set as low.

Note3: When TRSTn is high, the related debug interface pins (GPIO36 ~ GPIO39) must not be used as GPIO function.

2.10 General-purpose IOs (GPIOs)

The SPD1148 can be configured to support as many as 31 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

2.11 Timers and watchdogs

The SPD1148 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPD1148 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPD1148 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.12 UART

The SPD1148 has an UART module that are functionally compatible with the 16550A and 16750 industry standards. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 12.5 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.13 I²C

The I²C bus interface complies with the common I²C protocol and can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I²C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 50 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

2.15 ADC

A 14-bit analog-to-digital converter is embedded into SPD1148 and has up to 9 external channels. In addition, the temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed internally. The ADC core has three independent built-in sample-and-hold (S/H) blocks. Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 14-bit resolution
- 140 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Triple-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external source
- ADC external channel input open and short detection for safety

Please see Table 16 for ADC characteristics.

2.16 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into MCU portion of SPD1148 and share up to 9 input channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains for general purpose PGAs
  Differential mode: 2, 4, 8, 16, 24, 32, 48, 64; Single-ended mode: 1, 2, 4, 8, 12, 16, 24, 32.
- Differential mode optimized for motor current sensing using on-board resistive level shifters
- Settling time: 400 ns to 800 ns

Please see Table 17 for PGA characteristics.

2.18 Analog comparators

The SPD1148 has ten high-speed comparators. Each comparator uses the internal DAC as reference for monitoring PGA inputs or outputs. Two comparators are designed for each PGA: one is monitoring whether the voltage is too high, the other is monitoring whether the voltage is too low. The extra two pairs of comparators are reserved for additional applications. The comparator output is routed to the PWM Trip-Zone modules. Additionally, each comparator can implement the phase comparison for motor commutation. The detail channel selection can be referred to Technical Reference Manual.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter
- Phase comparison

Please see Table 18 and Table 19 for analog comparator and DAC characteristics.

2.19 PWMs

The SPD1148 integrates six PWM modules and supports 12 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules

- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.20 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1148 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.21 Cyclic redundancy check (CRC)

The SPD1148 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Five CRC standard polynomials supported

2.22 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128-, 192-, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

2.23 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPD1148 certain security feature.

2.24 SIO

SPD1148 has implemented an SIO module, which is based on a Spintrol patented technology. It has

programmable capability that can convert the SIO module into pre-defined communication module. Currently the SIO can be used as UART, SPI, I2C and CAN once it is programmed through initialization. There will be more features added in short time.

2.25 Power management module

SPD1148 integrates power management module including Buck DC-DC providing 3.3V power rail for the MCU and LDO providing 10V for pre-driver.

The Buck module converts main input supply VBAT to DVDD rail (typically 3.3V) for powering MCU. The Buck uses no external power FET or diode or external compensation resistors and capacitors, which saves cost and board space. Inductor value is 10uH and output cap is 10uF as shown in the typical application diagram in Figure 3. The Buck will start operating when VBAT voltage is higher than 4.56V and shut down when VBAT voltage drops below 4.15V. Typical switching frequency for LV buck is 1.2MHz, and typical current limit value is 500mA.

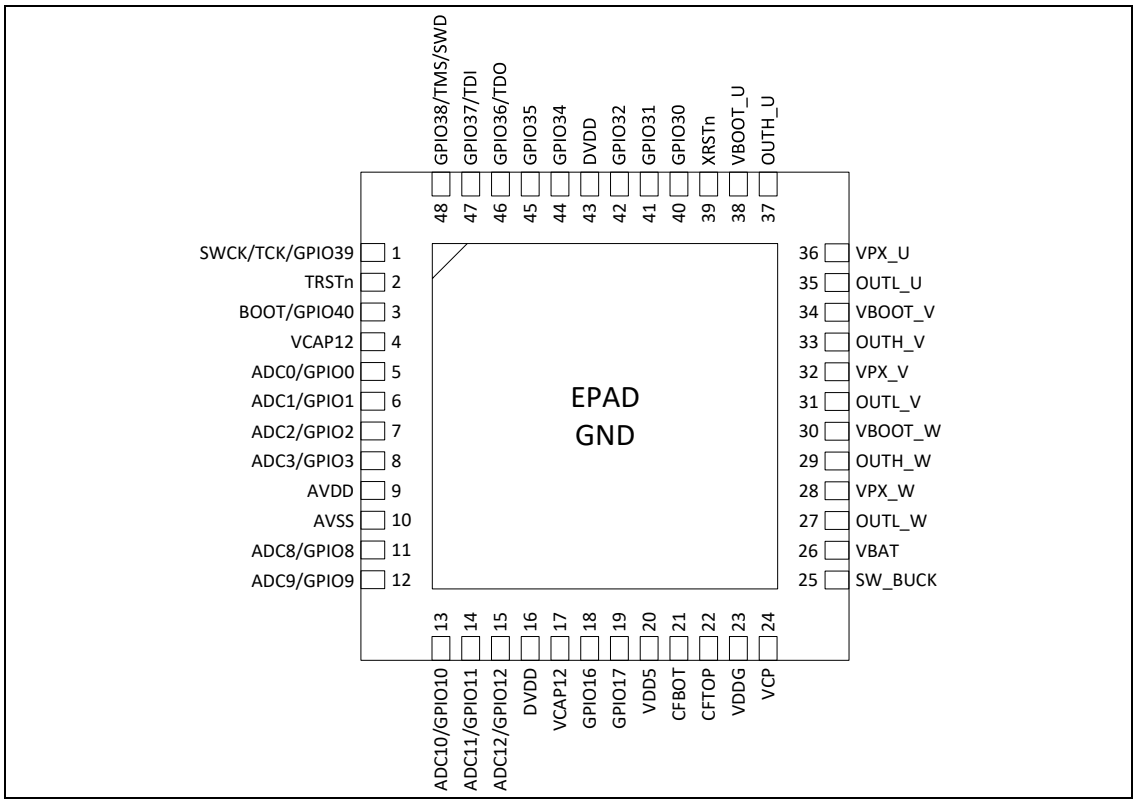
2.26 Pre-Driver system

Pre-Driver system consists of a three low- and high-side pre-drivers which can drive the three phases of low- and high-side external power NFET's or IGBT's. The voltage range of each low-side pre-driver is zero to VDDG, which is typically 10V and can be programmed. The embedded charge pump guarantees 100% duty cycle, i.e. allows high-side of each phase to be on indefinitely without loss of charge on the high-side pre-driver stage. Non-overlap time is built in to prevent high side and low side power FET to turn on at the same time even in case of overlapping input PWM command. VDS monitor is used to observe the Drain to Source voltage of the turned-on external power FET and compare it to pre-set programmable reference. When excessive current flows through the power FET, fault will be trigger to stop the Motor PWM signal through PWM trip zone. The VDS monitors are also very useful when detecting motor short to power/ground.

3 Pinout and pin description

3.1 QFN48

Figure 4. SPD1148 QFN48 pin-out



(1) The above figure shows the package top view.

(2) Note: there is no need to connect the two VCAP12 pins on the PCB boards.

(3) Note: when TRSTn is HIGH, GPIO36 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 1. SPD1148 QFN48 pin definitions

Pin	Signal	Type(1)	Description
1	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG test clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SIO0_17	O	SIO0 input/output 17
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
2	TRSTn	I	JTAG test reset pin, reset the JTAG test when low

Table 1. SPD1148 QFN48 pin definitions (continued)

Pin	Signal	Type(1)	Description
3	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
	SIO0_0	I/O	SIO0 input/output 0
4	VCAP12	S	1.2V power
5	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
6	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
7	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
8	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
9	AVDD	S	Analog power
10	AVSS	S	Analog ground
11	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
12	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
13	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output

Table 1. SPD1148 QFN48 pin definitions (continued)

Pin	Signal	Type[1]	Description
14	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
15	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	I2C_SCL	I/O	I^2C clock
16	DVDD	S	Digital power
17	VCAP12	S	1.2V power
18	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
19	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input/output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SIO0_13	I/O	SIO0 input/output 13
20	VDD5	S	5V auxiliary supply
21	CFBOT	S	Charge pump flying capacitor bottom plate voltage
22	CFTOP	S	Charge pump flying capacitor top plate voltage
23	VDDG	S	VDDG supply pin for Pre-Driver
24	VCP	S	Charge pump output
25	SW_BUCK	S	Buck switching pin, connect to 10uH inductor
26	VBAT	S	VBAT supply pin
27	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive
28	VPX_W	O	Pre-Driver W-Phase power FET switching node
29	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive
30	VBOOT_W	S	Pre-Driver W-Phase bootstrap pin
31	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
32	VPX_V	O	Pre-Driver V-Phase power FET switching node
33	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive

Table 1. SPD1148 QFN48 pin definitions (continued)

Pin	Signal	Type(1)	Description
34	VBOOT_V	S	Pre-Driver V-Phase bootstrap pin
35	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
36	VPX_U	O	Pre-Driver U-Phase power FET switching node
37	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
38	VBOOT_U	S	Pre-Driver U-Phase bootstrap pin
39	XRSTn	I	Device reset pin, reset the device when low
40	GPIO30	I/O	General-purpose input/output 30
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	COMP3H	O	Comparator COMP3H result output
	PWM3A	O	PWM3 output A
	PWM0A	O	PWM0 output A
	SIO0_8	I/O	SIO0 input/output 8
41	GPIO31	I/O	General-purpose input/output 31
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	COMP3L	O	Comparator COMP3L result output
	PWM3B	O	PWM3 output B
	PWM0B	O	PWM0 output B
	SIO0_9	I/O	SIO0 input/output 9
42	GPIO32	I/O	General-purpose input/output 32
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
	PWM4A	O	PWM4 output A
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	SIO0_10	I/O	SIO0 input/output 10
43	DVDD	S	Digital power
44	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12

Table 1. SPD1148 QFN48 pin definitions (continued)

Pin	Signal	Type(1)	Description
45	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
46	GPIO36	I/O	General-purpose input/output 36
	TDO	O	JTAG data output
	UART_RXD	I	UART receive data
	SPI_SCLK	I/O	SPI clock input/output
	PWM5A	O	PWM5 output A
	PWM1A	O	PWM1 output A
	I2C_SDA	I/O	I^2C data
	SIO0_14	I/O	SIO0 input/output 14
	Note: when TRSTn is HIGH, this pin always works as TDO and can't be configured as other functions.		
47	GPIO37	I/O	General-purpose input/output 37
	TDI	I	JTAG data input
	UART_TXD	O	UART transmit data
	SPI_SFRM	I/O	SPI frame signal
	PWM5B	O	PWM5 output B
	PWM1B	O	PWM1 output B
	I2C_SCL	I/O	I^2C clock
	SIO0_15	I/O	SIO0 input/output 15
	Note: when TRSTn is HIGH, this pin always works as TDI and can't be configured as other functions.		
48	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		

(1) I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

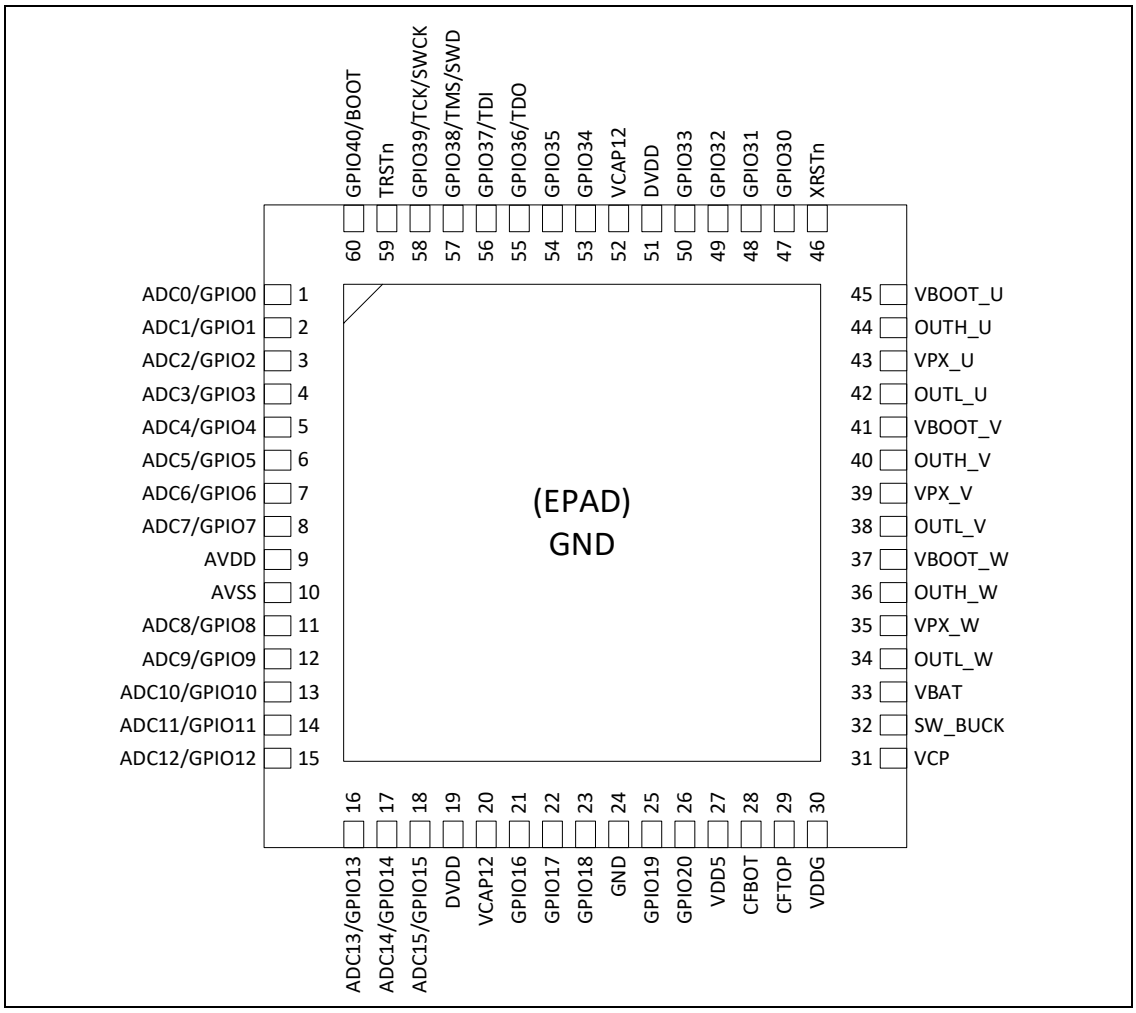
(2) EPWRTZO signal is logic OR of EPWRTZ0O signal and EPWRTZ1O signal.

(3) All GPIO pins can be configured as ECAP input.

(4) All GPIO pins (except GPIO36 and GPIO37) can be configured as ECAP output.

3.2 QFN60

Figure 5. SPD1148 QFN60 pin-out



(1) The above figure shows the package top view.

(2) Note: there is no need to connect the two VCAP12 pins on the PCB boards.

(3) Note: when TRSTn is HIGH, GPIO36 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 2. SPD1148 QFN60 pin definitions

Pin	Signal	Type(1)	Description
1	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
2	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
3	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output

Table 2. SPD1148 QFN60 pin definitions (continued)

Pin	Signal	Type[1]	Description
4	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
5	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
6	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
7	GPIO6	I/O	General-purpose input/output 6
	ADC6	AI	ADC channel 6 input
8	GPIO7	I/O	General-purpose input/output 7
	ADC7	AI	ADC channel 7 input
9	AVDD	S	Analog power
10	AVSS	S	Analog ground
11	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
12	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
13	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
14	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
15	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	I2C_SCL	I/O	I^2C clock

Table 2. SPD1148 QFN60 pin definitions (continued)

Pin	Signal	Type[1]	Description
16	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	I2C_SDA	I/O	I^2C data
17	GPIO14	I/O	General-purpose input/outpu14
	ADC14	AI	ADC channel 14 input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
18	GPIO15	I/O	General-purpose input/output 5
	ADC15	AI	ADC channel 15 input
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
19	DVDD	S	Digital power
20	VCAP12	S	1.2V power
21	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
22	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input/output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SIO0_13	I/O	SIO0 input/output 13
23	GPIO18	I/O	General-purpose input/output 18
	PWM3A	O	PWM3 output A
	COMP3H	O	Comparator COMP3H result output
	PWM0A	O	PWM0 output A
	SIO0_14	I/O	SIO0 input/output 14
24	GND	S	Ground
25	GPIO19	I/O	General-purpose input/output 19
	PWM4A	O	PWM4 output A
	PWM3B	O	PWM3 output B
	COMP3L	O	Comparator COMP3L result output
	PWM1A	O	PWM1 output A
	PWM0B	O	PWM0 output B
	SIO0_15	I/O	SIO0 input/output 15

Table 2. SPD1148 QFN60 pin definitions (continued)

Pin	Signal	Type(1)	Description
26	GPIO20	I/O	General-purpose input/output 20
	COMP4H	O	Comparator COMP4H result output
	PWM2A	O	PWM2 output A
	PWM1A	O	PWM1 output A
	SIO0_16	I/O	SIO0 input/output 16
27	VDD5	S	5V auxiliary supply
28	CFBOT	S	Charge pump flying capacitor bottom plate voltage
29	CFTOP	S	Charge pump flying capacitor top plate voltage
30	VDDG	S	VDDG supply pin for Pre-Driver
31	VCP	S	Charge pump output
32	SW_BUCK	S	Buck switching pin, connect to 10uH inductor
33	VBAT	S	VBAT supply pin
34	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive
35	VPX_W	O	Pre-Driver W-Phase power FET switching node
36	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive
37	VBOOT_W	S	Pre-Driver W-Phase bootstrap pin
38	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
39	VPX_V	O	Pre-Driver V-Phase power FET switching node
40	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive
41	VBOOT_V	S	Pre-Driver V-Phase bootstrap pin
42	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
43	VPX_U	O	Pre-Driver U-Phase power FET switching node
44	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
45	VBOOT_U	S	Pre-Driver U-Phase bootstrap pin
46	XRSTn	I	Device reset pin, reset the device when low
47	GPIO30	I/O	General-purpose input/output 30
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	COMP3H	O	Comparator COMP3H result output
	PWM3A	O	PWM3 output A
	PWM0A	O	PWM0 output A
	SIO0_8	I/O	SIO0 input/output 8
48	GPIO31	I/O	General-purpose input/output 31
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	COMP3L	O	Comparator COMP3L result output
	PWM3B	O	PWM3 output B
	PWM0B	O	PWM0 output B
	SIO0_9	I/O	SIO0 input/output 9

Table 2. SPD1148 QFN60 pin definitions (continued)

Pin	Signal	Type(1)	Description
49	GPIO32	I/O	General-purpose input/output 32
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
	PWM4A	O	PWM4 output A
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	SIO0_10	I/O	SIO0 input/output 10
50	GPIO33	I/O	General-purpose input/output 33
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	PWM4B	O	PWM4 output B
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
	SIO0_11	I/O	SIO0 input/output 11
51	DVDD	S	Digital power
52	VCAP12	S	1.2V power
53	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12
54	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
55	GPIO36	I/O	General-purpose input/output 36
	TDO	O	JTAG data output
	UART_RXD	I	UART receive data
	SPI_SCLK	I/O	SPI clock input/output
	PWM5A	O	PWM5 output A
	PWM1A	O	PWM1 output A
	I2C_SDA	I/O	I^2C data
	SIO0_14	I/O	SIO0 input/output 14
	Note: when TRSTn is HIGH, this pin always works as TDO and can't be configured as other functions.		

Table 2. SPD1148 QFN60 pin definitions (continued)

Pin	Signal	Type(1)	Description
56	GPIO37	I/O	General-purpose input/output 37
	TDI	I	JTAG data input
	UART_TXD	O	UART transmit data
	SPI_SFRM	I/O	SPI frame signal
	PWM5B	O	PWM5 output B
	PWM1B	O	PWM1 output B
	I2C_SCL	I/O	I^2C clock
	SIO0_15	I/O	SIO0 input/output 15
	Note: when TRSTn is HIGH, this pin always works as TDI and can't be configured as other functions.		
57	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
58	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG test clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SIO0_17	O	SIO0 input/output 17
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
59	TRSTn	I	JTAG test reset pin, reset the JTAG test when low
60	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
	SIO0_0	I/O	SIO0 input/output 0

(1) I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

(2) EPWRTZO signal is logic OR of EPWRTZ0O signal and EPWRTZ1O signal.

(3) All GPIO pins can be configured as ECAP input.

(4) All GPIO pins (except GPIO36 and GPIO37) can be configured as ECAP output.

3.3 PGA input channel selection

For the three on-MCU PGA's, each PGA has two 1-of-8 multiplexers (MUX) for input channel selection, one is for positive input (PGAx_P, x = 0,1,2) and the other is for negative input (PGAx_N, x = 0,1,2). The input channel selection table is shown below.

Table 3. PGA input channel selection

MUX Value	PGA0_P	PGA0_N	PGA1_P	PGA1_N	PGA2_P	PGA2_N
7	ADC4	ADC3	ADC9	ADC1	ADC14	ADC15
6	ADC10	ADC5	ADC10	ADC11	ADC12	ADC13
5	ADC8	ADC9	ADC8	ADC10	ADC8	ADC11
4	ADC6	ADC7	ADC2	ADC3	ADC4	ADC5
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
2	DAC2	DAC3	ATEST	VDD12	TSEN1(1)	TSEN0(1)
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
0	GND	GND	GND	GND	GND	GND

(1) TSEN0 is output 0 of T-Sensor and TSEN1 is output 1 of T-Sensor.

3.4 GPIO pin function and state after reset

Table 4. GPIO pin function and state after reset

Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
GPIO4	ADC4	Floating
GPIO5	ADC5	Floating
GPIO6	ADC6	Floating
GPIO7	ADC7	Floating
GPIO8	ADC8	Floating
GPIO9	ADC9	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO12	ADC12	Floating
GPIO13	ADC13	Floating
GPIO14	ADC14	Floating
GPIO15	ADC15	Floating
GPIO16	GPIO16	Floating
GPIO17	GPIO17	Floating
GPIO18	GPIO18	Floating
GPIO19	GPIO19	Floating
GPIO20	GPIO20	Floating

Pin Name	Default Function	Default State
~~GPIO21~~	~~GPIO21~~	Floating
~~GPIO22~~	~~GPIO22~~	Floating
~~GPIO23~~	~~GPIO23~~	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Floating
GPIO26	GPIO26	Floating
GPIO27	GPIO27	Floating
GPIO28	GPIO28	Floating
GPIO29	GPIO29	Floating
GPIO30	GPIO30	Floating
GPIO31	GPIO31	Floating
GPIO32	GPIO32	Floating
GPIO33	GPIO33	Floating
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO36	GPIO36	Floating
GPIO37	GPIO37	Floating
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40/BOOT	Pull up

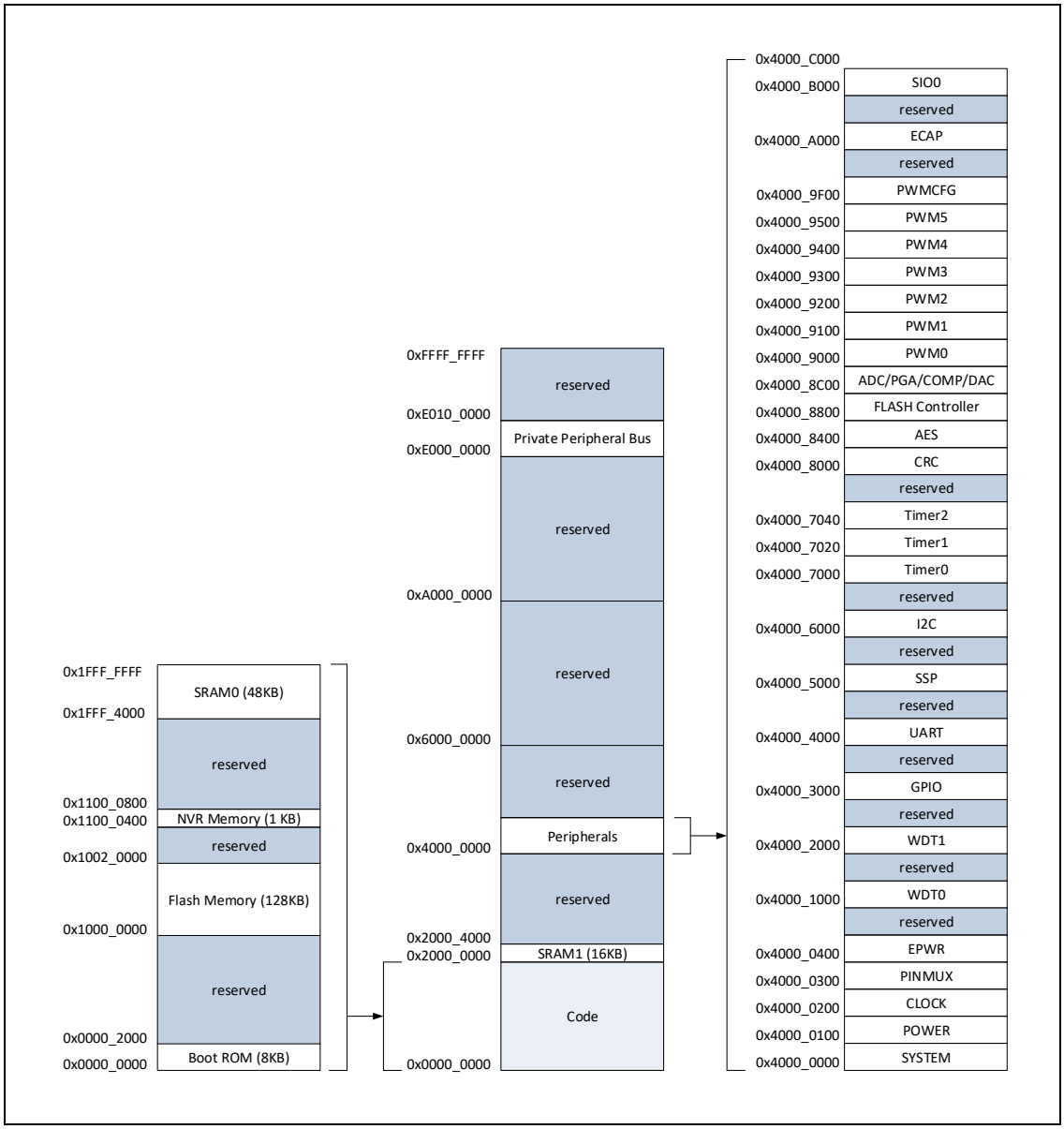
(1) InSPD1148, GPIO24~ GPIO29 are internally connected to the high voltage module, and not bonded out to the external pin.

(2) In SPD1148, the GPIOs with strikeout are not bonded out to the external pin.

4 Memory mapping

The memory map of SPD1148 is shown in Figure 6.

Figure 6. Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5. Absolute maximum ratings (1)(2)

Symbol	Parameter	Min	Max	Unit
VBAT	Pre-Driver and Buck supply voltage, with respect to V_{SS}	5.5	44	V
V_{DDG}	Pre-Driver low-side gate voltage, with respect to V_{SS}	5.5	18	V
V_{BOOT}	Pre-Driver high-side floating power level, to V_{SS}	-	56	V
V_{BS}	Pre-Driver high side power rail (V_{BOOT} - V_{PX})	-0.3	20	V
V_{CP}	Pre-Driver charge pump output voltage	VBAT-0.6	VBAT+20	V
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_A	Ambient temperature(3)	-40	+105	°C
T_{stg}	Storage temperature(3)	-65	+150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
VBAT	Pre-Driver supply voltage	-	5.5	24	42	V
V_{VDDG}	Pre-Driver low-side gate voltage	-	5.5	10	18	V
V_{BOOT}	Pre-Driver high-side floating power level	-	4.8	-	56	V
V_{DD}	Supply voltage	-	2.97	3.3	3.63	V
V_{SS}	Supply ground	-	-	0	-	V
V_{DDA}	Analog supply voltage	-	2.97	3.3	3.63	V
V_{SSA}	Analog ground	-	-	0	-	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current for GPIO when $V_{OH} = V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current for GPIO when $V_{OL} = V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
T_J	Junction temperature	-	-40	-	+125	°C
T_A	Ambient temperature		-40	-	+105	°C

5.3 I/O Electrical characteristics

Table 7. I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	VDD-0.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = 0 V	-	-	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = V_{DD}	-	-	2	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	-	41	-	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DD}	-	42	-	kΩ

5.4 Power consumption summary

Typical current consumption

In operational mode, the SPD1148 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected
- All peripherals (including analog module) are enabled, except SIO module
- All peripheral clocks are as fast as HCLK (frequency division is Zero), except SSP (Max 50 MHz) I2C (Max 50 MHz), PCLK (Max 50 MHz)
- All clock modules are enabled
- Select PLL clock as system clock source

In idle mode, the SPD1148 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected
- All peripherals (including analog module) are clocked off or disabled
- Clock modules (PLL, RCO0 and XO) are disabled
- Select RCO1 as system clock source

In global deep sleep mode, the SPD1148 is placed under the following conditions:

- The Buck and Pre-Driver LDO are disabled, thus no power supply for MCU and Pre-Driver
- All the control blocks are disabled except reset monitoring logic used for wake-up command

In MCU-only deep sleep mode, the SPD1148 is placed under the following conditions:

- The Buck is on
- All I/O pins are in input mode and left unconnected
- All peripherals (including analog module) are clocked off or disabled
- Clock modules (PLL, RCO1 and XO) are disabled
- 1.2V LDO is shut down to 0V.

The typical current consumption of SPD1148 measured from VBAT is shown in Table 8 and Table 9. The operational current consumption over various HCLK frequency is shown in Figure 7.

Table 8. SPD1148 typical current consumption (Run in FLASH)

Mode	Conditions			VBAT = 12V	VBAT = 24V	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}			
Operational	200 MHz(2)	50 MHz	200 MHz	25.3	13.6	mA
	175 MHz(2)	43.75 MHz	175 MHz	24.1	13.1	mA
	168 MHz(2)	42 MHz	168 MHz	23.7	12.9	mA
	150 MHz(2)	50 MHz	150 MHz	22.7	12.5	mA
	125 MHz(2)	41.67 MHz	125 MHz	21.5	11.9	mA
	100 MHz	50 MHz	100 MHz	20.3	11.2	mA
	75 MHz	37.5 MHz	75 MHz	19.0	10.6	mA
	50 MHz	50 MHz	50 MHz	17.8	9.95	mA
	32 MHz	32 MHz	32 MHz	16.7	9.36	mA
	25 MHz	25 MHz	25 MHz	16.2	9.1	mA
Idle (Pre-Driver enabled)	2.2 MHz	2.2 MHz	-	5.2	4.3	mA
Idle	2.2 MHz	2.2 MHz	-	3.1	2.2	mA
Deep Sleep	-	-	-	7	9	uA

(1) Typical values are measured at T_A = 25 °C.

(2) SIO module clock frequency is f_{HCLK} / 2.

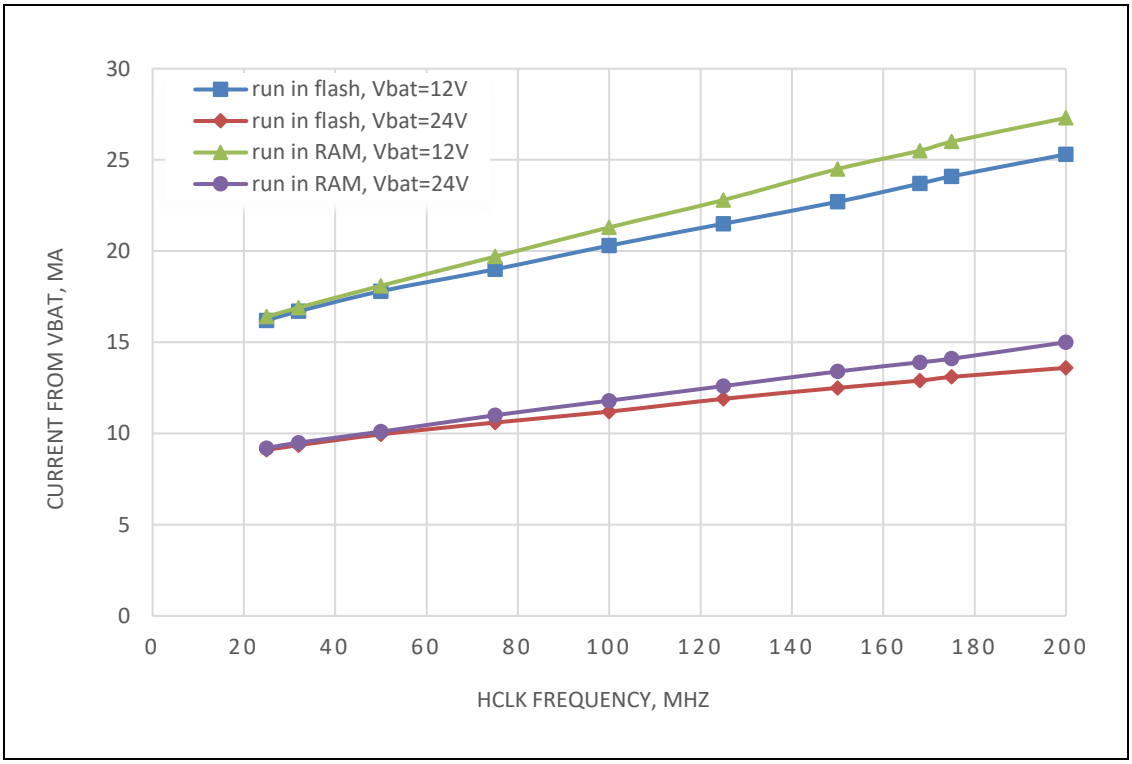
Table 9. SPD1148 typical current consumption (Run in RAM)

Mode	Conditions			VBAT = 12V	VBAT = 24V	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}			
Operational	200 MHz(2)	50 MHz	200 MHz	27.3	15.0	mA
	175 MHz(2)	43.75 MHz	175 MHz	26.0	14.1	mA
	168 MHz(2)	42 MHz	168 MHz	25.5	13.9	mA
	150 MHz(2)	50 MHz	150 MHz	24.5	13.4	mA
	125 MHz(2)	41.67 MHz	125 MHz	22.8	12.6	mA
	100 MHz	50 MHz	100 MHz	21.3	11.8	mA
	75 MHz	37.5 MHz	75 MHz	19.7	11.0	mA
	50 MHz	50 MHz	50 MHz	18.1	10.1	mA
	32 MHz	32 MHz	32 MHz	16.9	9.5	mA
	25 MHz	25 MHz	25 MHz	16.4	9.2	mA
Idle	2.2 MHz	2.2 MHz	-	3.1	2.2	mA

(1) Typical values are measured at T_A = 25 °C.

(2) SIO module clock frequency is f_{HCLK} / 2.

Figure 7. Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 10. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

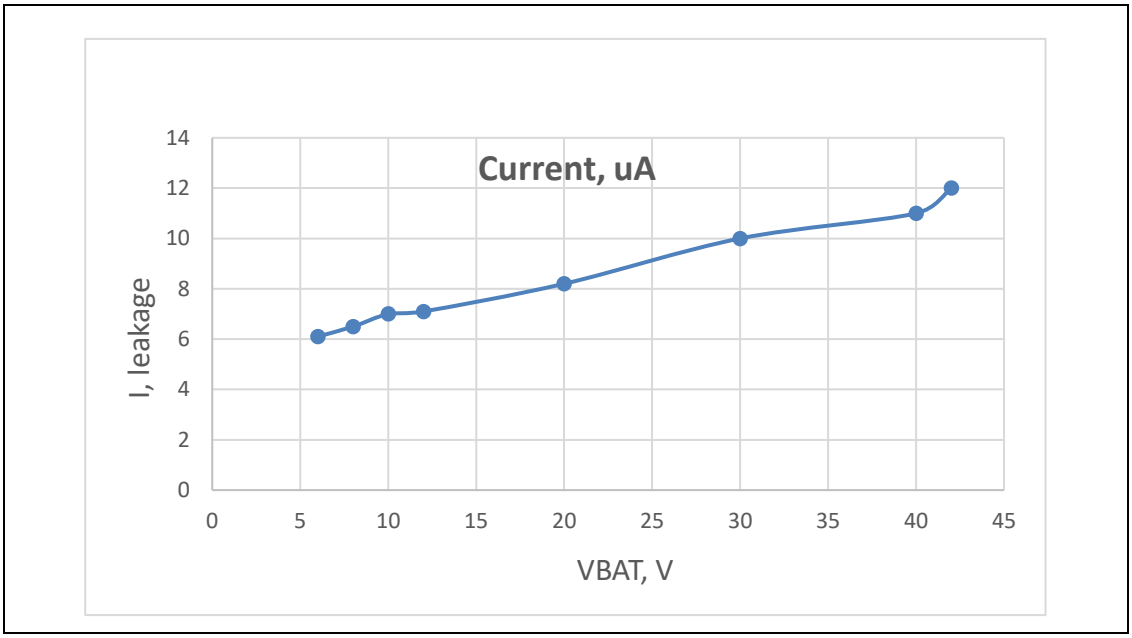
Table 10. Peripheral current consumption

Peripherals(1)		Conditions	Typ(2)	Unit
BOD		Select RCO0 as system clock source; All other peripherals are in default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	0.1	mA
ADC	Analog (3)	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 128 MHz, f_{PCLK} = 32 MHz, f_{PLL} = 128 MHz	16.52	mA
	Digital		0.31	mA
T-Sensor			0.16	mA
PGA (4)			4.10	mA
DAC			0.18	mA
Comparator			0.08	mA
UART		UART clock 200MHz, 256000 bps	0.416	mA
I2C		I2C clock 50MHz, 3.4Mbps	0.316	mA
SSP		SSP clock 50MHz, 50Mbps	0.361	mA
PWM		PWM clock 200MHz	1.471	mA
ECAP		ECAP clock 200MHz	0.329	mA
WDT		WDT clock 200MHz	0.245	mA
TMR		TMR clock 200MHz	0.385	mA
SIO		SIO clock 100MHz	6.63	mA
FLASH		HCLK clock 200MHz	0.772	mA
XO		HCLK is from 200MHz PLL, which takes RCO0 as input	0.616	mA
RCO		HCLK is from 200MHz PLL, which takes XO as input	0.313	mA
PLL		XO as HCLK source, f_{PLL} = 32 MHz	1.153	mA

(1) For peripherals with multiple instances, the current quoted is for single modules. For example, the 4.10 mA value quoted for PGA is for one PGA module. So the total 3 PGA module current is 12.30mA.
(2) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(3) ADC analog current contain ADC analog module, bandgap and ADC reference buffer.
(4) The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

In the deep sleep mode power dissipation depends on the input voltage level VBAT. The dependency of deep sleep mode current on VBAT is shown in Figure 8.

Figure 8. Deep sleep mode leakage vs. VBAT level



5.5 Internal 1.2V regulator characteristics

Table 11. Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply	-	2.97	3.3	3.63	V
VCAP12	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation	VCAP12(50mA load) -VCAP12(200mA load)	-	-	30	mV

Figure 9. Internal 1.2V regulator load regulation (T_A = 25 °C)

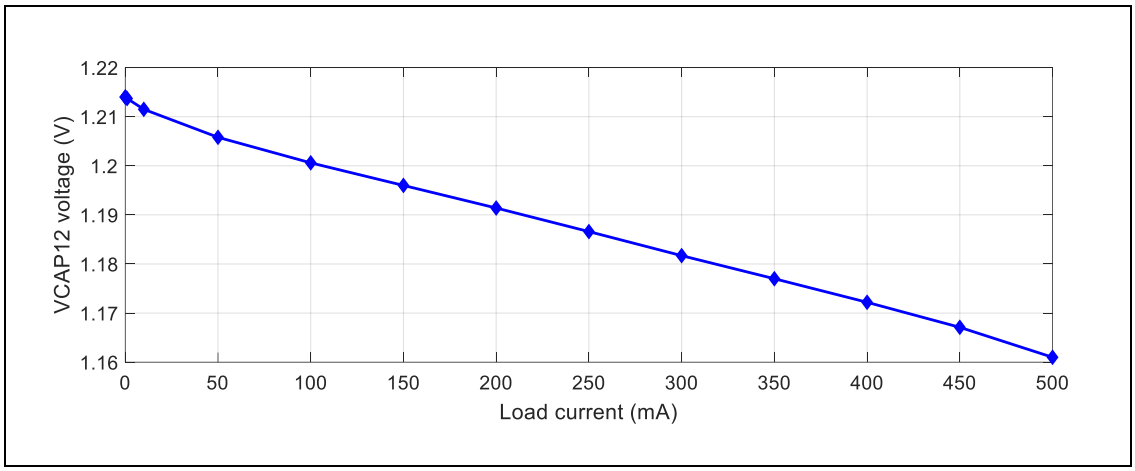
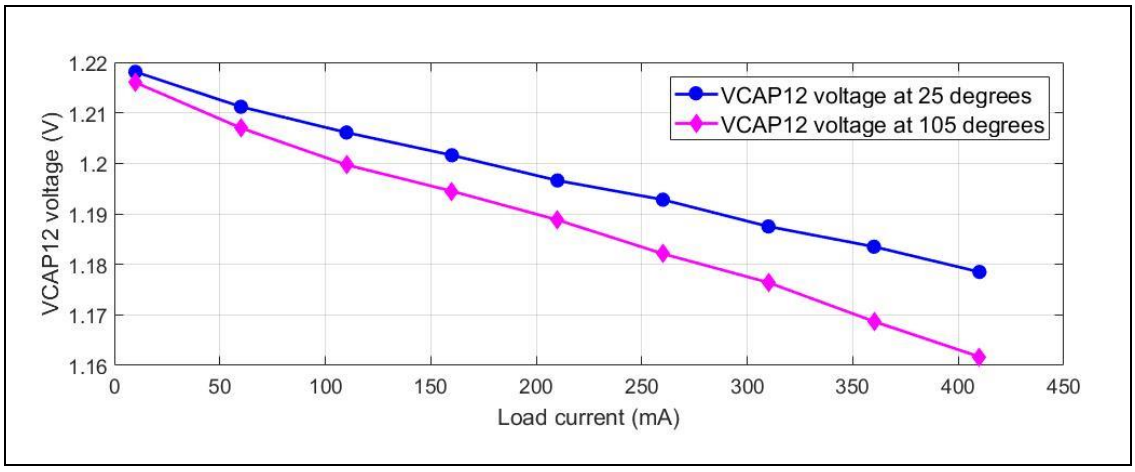


Figure 10. Internal 1.2V regulator load regulation with different temperature



5.6 BOD characteristics

Table 12. BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{DD33H_Asset}	VDD33 too high assert threshold	-	-	3.42	-	V
$V_{DD33H\_Deasset}$	VDD33 too high de-assert threshold	-	-	3.31	-	V
V_{DD33L_Asset}	VDD33 too low assert threshold		-	2.58	-	V
$V_{DD33L\_Deasset}$	VDD33 too low de-assert threshold		-	2.65	-	V
V_{DD12H_Asset}	VDD12 too high assert threshold		-	1.33	-	V
$V_{DD12H\_Deasset}$	VDD12 too high de-assert threshold		-	1.31	-	V
V_{DD12L_Asset}	VDD12 too low assert threshold(1)		-	0.94	-	V
$V_{DD12L\_Deasset}$	VDD12 too low de-assert threshold(1)		-	0.97	-	V

(1) The characteristics of VDD12 too low 0 and VDD12 too low 1 are the same.

5.7 RCO characteristics

Table 13. RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	32.00	32.064	MHz
ACC_{RCO}	RCO frequency accuracy (RCO frequency variation versus temperature)	T_J = -40~125 °C	-1	-	1	%

5.8 PLL characteristics

Table 14. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{VCO}	VCO frequency	-	400	500	600	MHz
F_{pfd}	Phase-Frequency Detector (PFD) input frequency	-	4	-	8	MHz
t_{LOCK}	Locking time		-	-	15	us

5.9 XO characteristics

Table 15. XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{XO}	XO frequency	-	1	-	66	MHz

The negative resistance of the on-chip crystal oscillator at different temperature is shown in Figure 11 ~ Figure 14. The loading capacitor CL_eff is defined as equivalent capacitance seen by the on-chip crystal.

Figure 11. The negative resistance of the on-chip crystal oscillator at 50℃

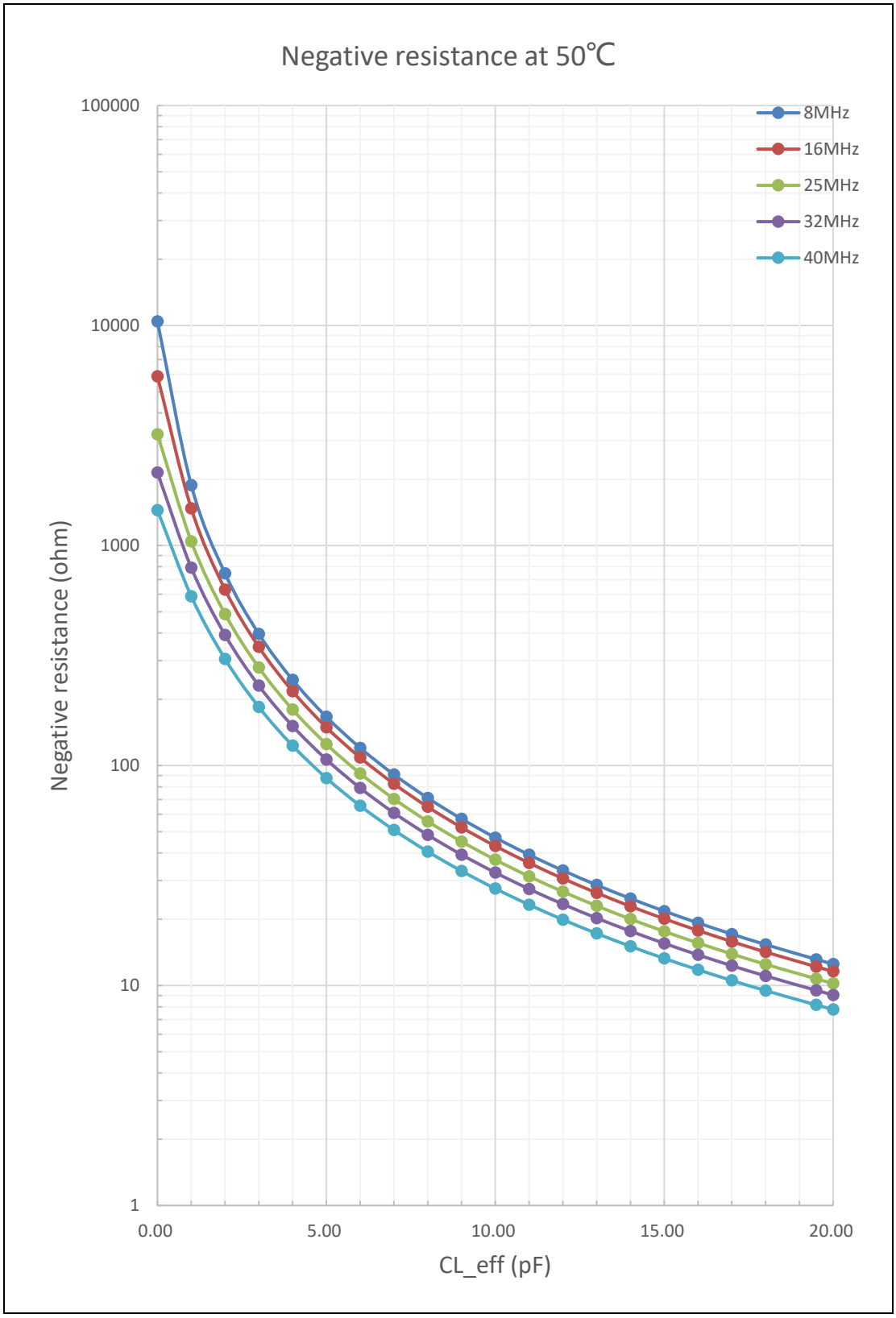


Figure 12. The negative resistance of the on-chip crystal oscillator at 85℃

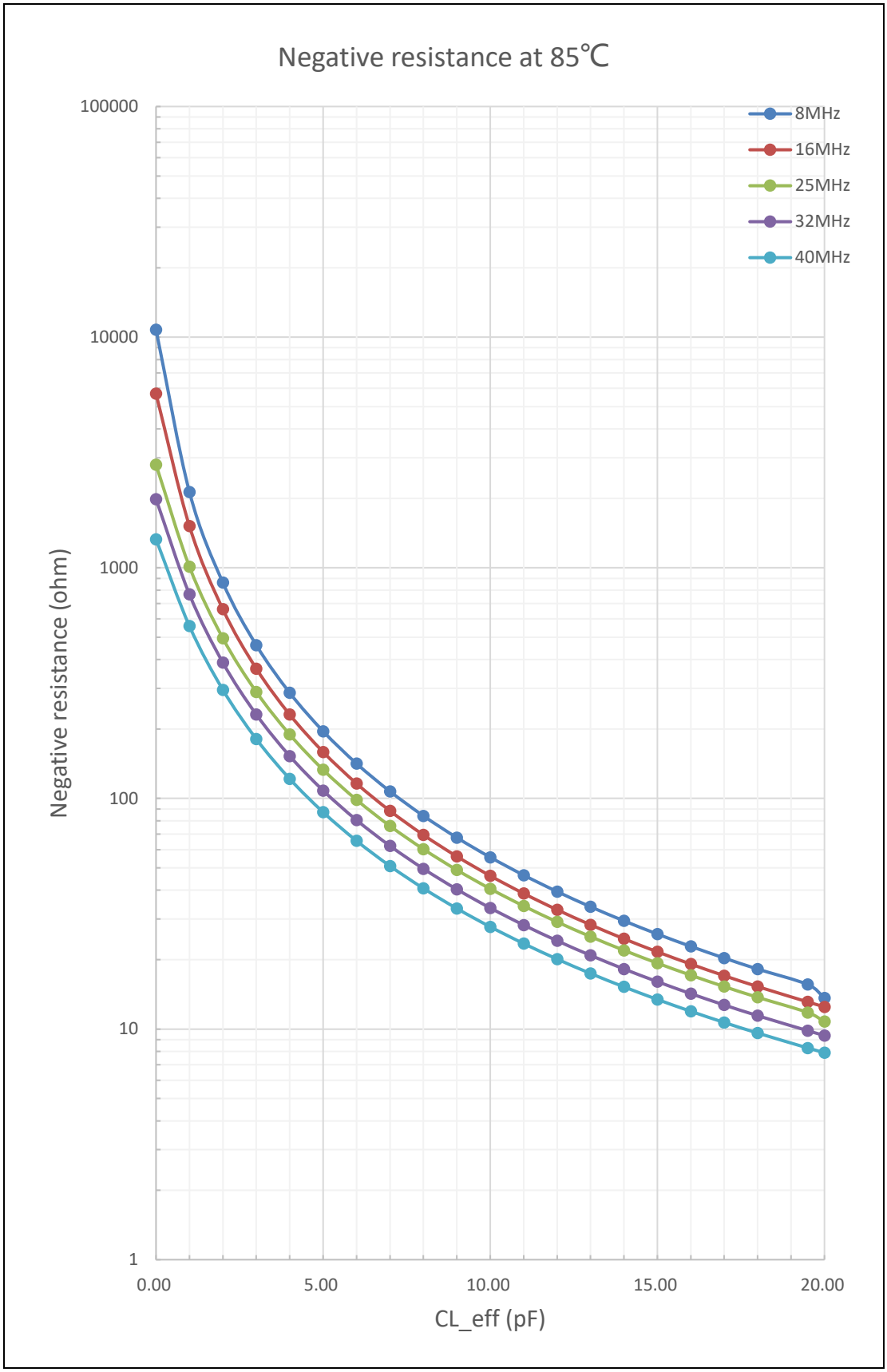


Figure 13. The negative resistance of the on-chip crystal oscillator at 100℃

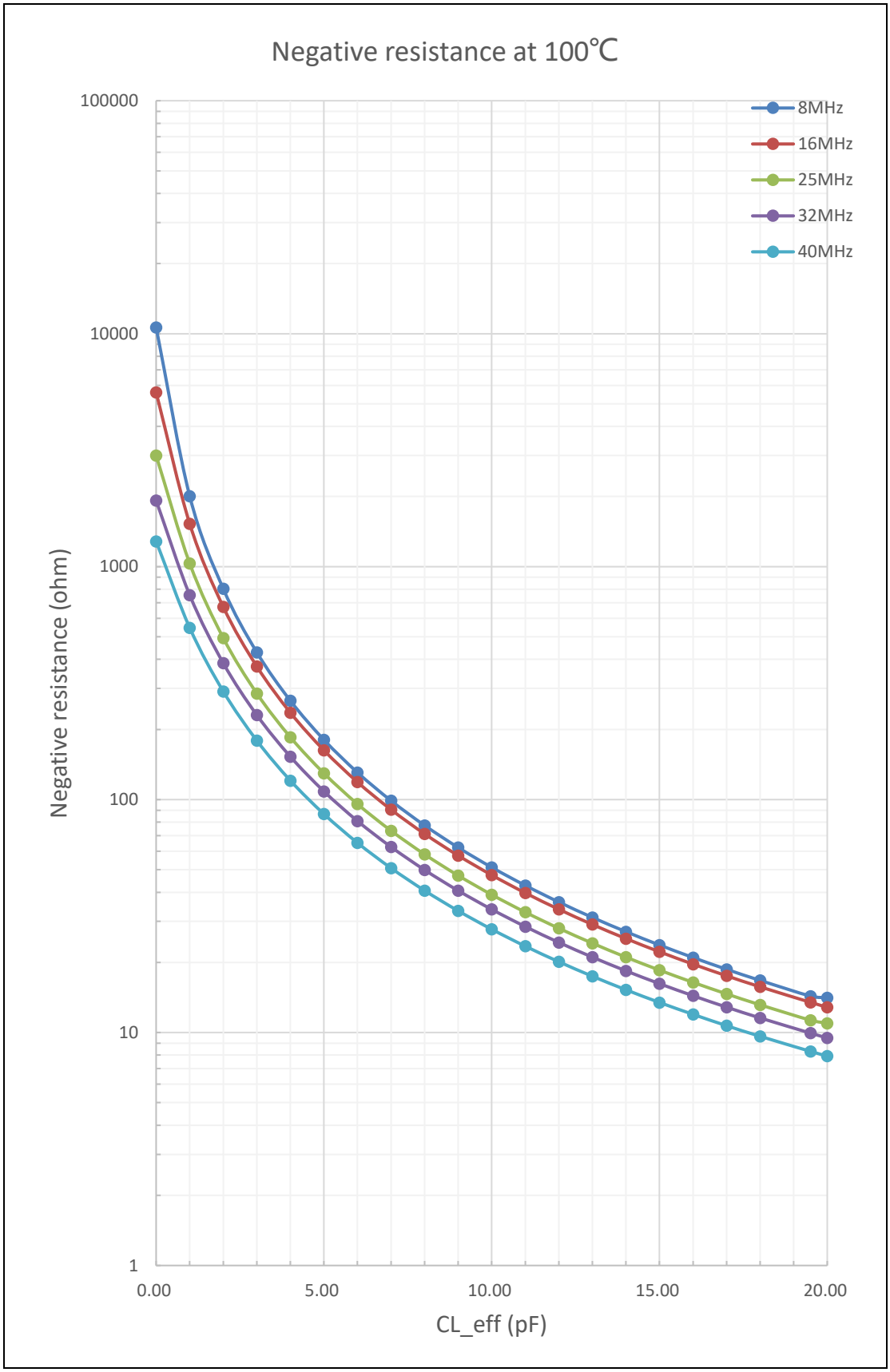
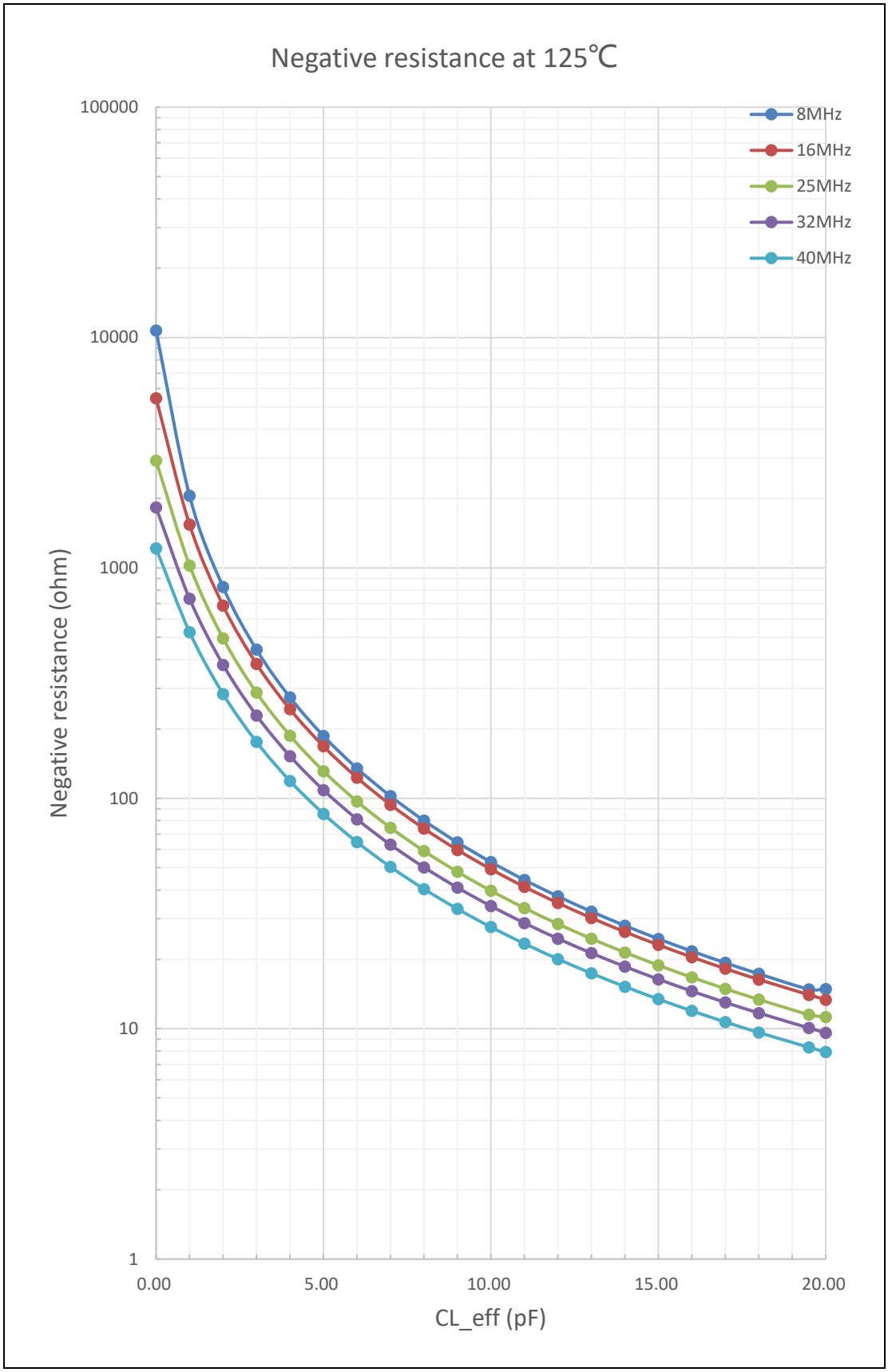


Figure 14. The negative resistance of the on-chip crystal oscillator at 125℃



5.10 14-bit ADC characteristics

Table 16. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	-	-	bit
F_S	Conversion speed(1)	-	-	-	4	MSPS
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{REF}	Reference voltage	-	1.194	1.2	1.206	V
I_{PAD}	Operational current	V_{DDA} = 3.3 V	-	17.1	21	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{OFF}	Offset error(2)	With calibration	-2	-	2	LSB
E_{GAIN}	Gain error(2)	With calibration	-4	-	4	LSB
E_{OFF2}	Channel to channel offset	-	-3	-	3	LSB
E_{GAIN2}	Channel to channel gain error	-	-5	-	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	-	-	26	-	ppm/°C
t_{PWRUP}	Power-up time	-	-	-	200	us
$ENOB_{DC}$	DC Noise Floor	-	-	12.0	-	bits
SNR	Signal-to-noise ratio	Fin = 100kHz, Amp = 0.94F_S, N = 8192	-	75.5	-	dB
THD	Total harmonic distortion		-	-85.0	-	dB
ENOB	Effective number of bits		-	12.2	-	bits
SFDR	Spurious free dynamic range		-	86.0	-	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	-	-	1.904(3)	-	°C/LSB
T_{OFFSET}	ADC output at 25 °C of the temperature sensor	-	-	162.138	-	LSB

(1) Sampling time = 110ns, conversion time = 140ns

(2) Offset and gain can be calibrated automatically by HW.

(3) Can be reduced to 0.24 °C/LSB by PGA.

5.11 PGA characteristics

Table 17. PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
R_{IN}	Input impedance	-	-	10	-	MΩ
G	Gain	Single-ended mode	1, 2, 4, 8, 12, 16, 24, 32			-
		Differential mode	2, 4, 8, 16, 24, 32, 48, 64			-
E_{GAIN}	Gain error	Differential Gain = 2	-0.5	-	0.5	%
		Differential Gain = 64	-3	-	3	%
V_{OS}	Offset	-	-5	-	5	mV
T_{OFFSET}	Offset temperature drift	-	-	5	-	uV/°C
SR	Slew rate	Single mode and Loading is ADC sampling capacitor	-	20	-	V/us
		Differential mode and Loading is ADC sampling capacitor	-	40	-	V/us
GBW	Gain band width	Single gain = 1	-	40	-	MHz
		Single gain = 8	-	6.8	-	MHz
		Single gain = 32	-	1.7	-	MHz
		Differential gain = 2	-	20	-	MHz
		Differential gain = 16	-	3.4	-	MHz
		Differential gain = 64	-	0.8	-	MHz
t_{SETTLE}	Settle time	Differential gain = 2	-	170(1)	220	ns
		Differential gain = 16		400	600	ns
		Differential gain = 64	-	1600	2200	ns
SNR	Signal-to-noise ratio	Differential gain = 2 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	74.0	-	dB
THD	Total harmonic distortion		-	-78.0	-	dB
ENOB	Effective number of bits		-	11.6	-	bit
SFDR	Spurious free dynamic range		-	82.0	-	dB
SNR	Signal-to-noise ratio	Differential gain = 64 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	58.0	-	dB
THD	Total harmonic distortion		-	-80.0	-	dB
ENOB	Effective number of bits		-	9.4	-	bit
SFDR	Spurious free dynamic range		-	63.0	-	dB
I	Current consumption	Only one PGA	-	4.16	5.20	mA

(1) Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled with 1LSB (446uV), guarantee by design.

5.12 Analog comparator characteristics

Table 18. Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	Common mode input voltage = 1.65V	-10	-	10	mV
V_{HYST}	Hysteresis voltage(12mV)	-	-	13	-	mV
	Hysteresis voltage(24mV)		-	26	-	mV
	Hysteresis voltage(36mV)		-	42	-	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	-	-	50	-	ns

5.13 Internal 10-bit DAC characteristics

Table 19. DAC characteristics

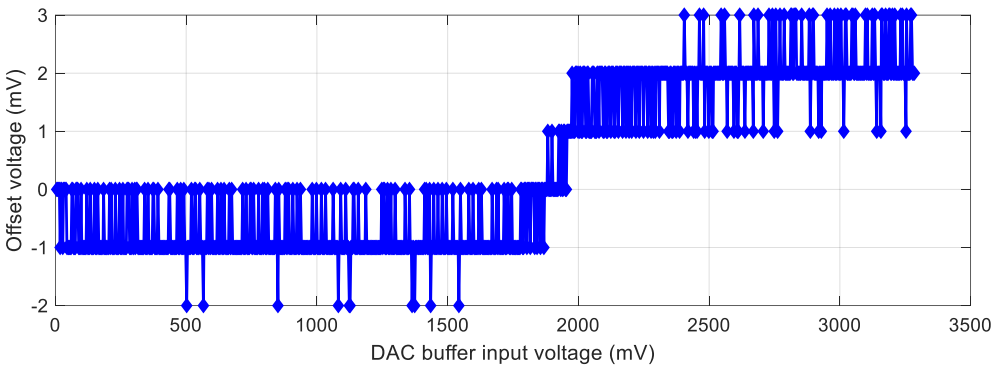
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N	Resolution	Monotonic	10	-	-	bit
V_{FS}	Full scale value	-	0	-	V_{DDA}	V
DNL	Differential linearity	-	-0.5	-	0.5	LSB
INL	Integral linearity	-	-1	-	1	LSB
E_{OFF}	Offset error	-	-	5	-	mV
t_{SETTLE}	DAC settling time	Design guarantee	-	-	1	us

5.14 DAC buffer characteristics

Table 20. DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
t_{SETTLE}	Settling time	Design guarantee	-	1	-	us
E_{OFF}	Offset error	-	-	3	-	mV
CL	Capacitor load	-	-	-	50	pF
RL	Resistor load	-	1	-	-	MΩ

Figure 15. DAC buffer offset over Input voltage



5.15 Flash memory characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 21. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	-	40	-	ns
t_{PROG}	Word (32-bit) program time	-	8	10	us
t_{SE}	Sector erase time	-	0.8	4	ms
t_{CE}	Chip erase time	-	8	10	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	10	-	years

5.16 Electrical sensitivity characteristics

Table 22. ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	Ambient temperature T_A = 25 °C		200	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	-	500	V
			Corner Pin	750	V

Table 23. Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C VBAT = 43V, VDDG = 20V, V_{DD} = 3.63V, VCAP12 = 1.32V	200	mA

5.17 Moisture sensitivity characteristics

Table 24. Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	-	Level 3	-

5.18 Thermal resistance characteristics

Table 25. Thermal resistance characteristics (QFN48 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	8.3064	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	31.5317	°C/W

(1) The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.19 SPI characteristics

Table 26. SPI characteristics

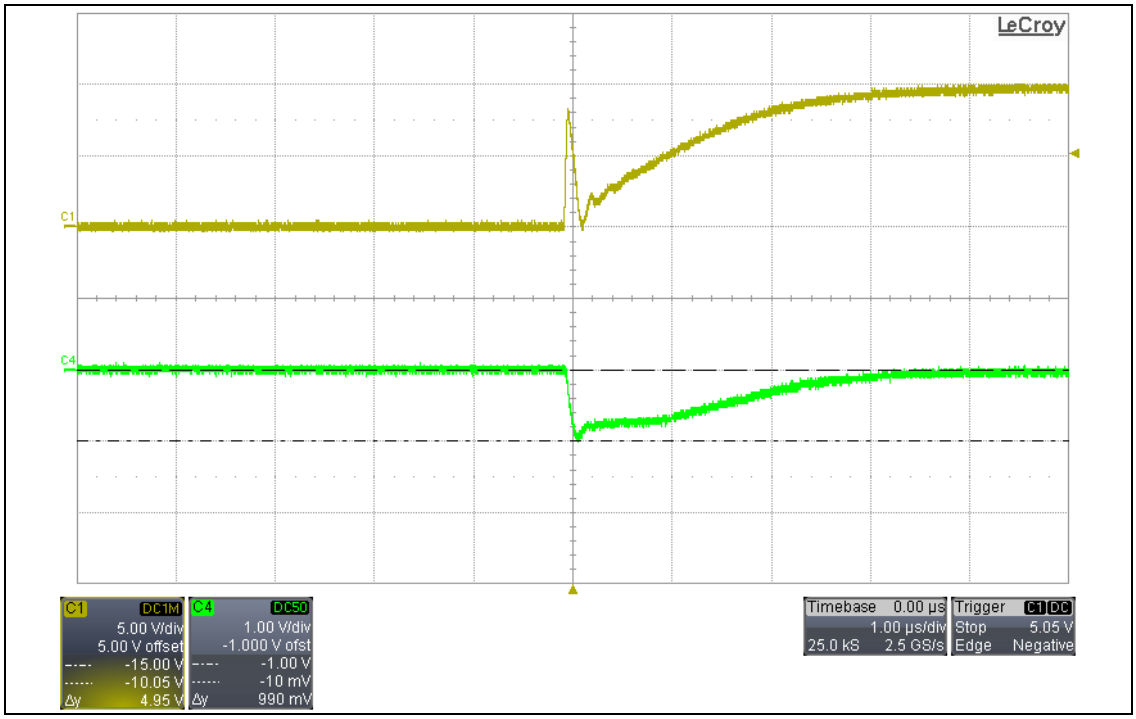
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	-	-	-	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	-	10	-	-	ns
$t_{SCLK(L)}$	SCLK clock low time	-	10	-	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(MO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(MI)}$	Data input setup time	-	6	-	-	ns
$t_{H(MI)}$	Data input hold time	-	2	-	-	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	-	5.6	-	-	ns
$t_{H(SFRM)}$	SFRM enable hold time	-	1.5	-	-	ns
$t_{A(SO)}$	Data output access time	-	4	-	10	ns
$t_{DIS(SO)}$	Data output disable time	-	4	-	10	ns
$t_{V(SO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(SO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(SI)}$	Data input setup time	-	6	-	-	ns
$t_{H(SI)}$	Data input hold time	-	2	-	-	ns

5.20 Pre-Driver characteristics

Table 27. Pre-Driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Input supply voltage	-	5.5	-	42	V
D_{MAX}	Maximum supported duty cycle	Charge pump will replenish bootstrap capacitor when high side is turned on	-	100	-	%
t_{DL}	Low-side propagation delay	1nF Capacitor as load	-	30	40	ns
t_{DH}	High-side propagation delay	1nF Capacitor as load	-	40	50	ns
Δt	High/Low side delay mismatch	-	-	-	12	ns
t_r	Rise time	1nF Capacitor as load	-	15	-	ns
t_f	Fall time	1nF Capacitor as load	-	15	-	ns
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagates	-10	-	-	V
I_{Source_Max}	Pre-Driver Max sourcing capability	-	-	1	-	A
I_{Sink_Max}	Pre-Driver Max sinking capability	-	-	1.3	-	A

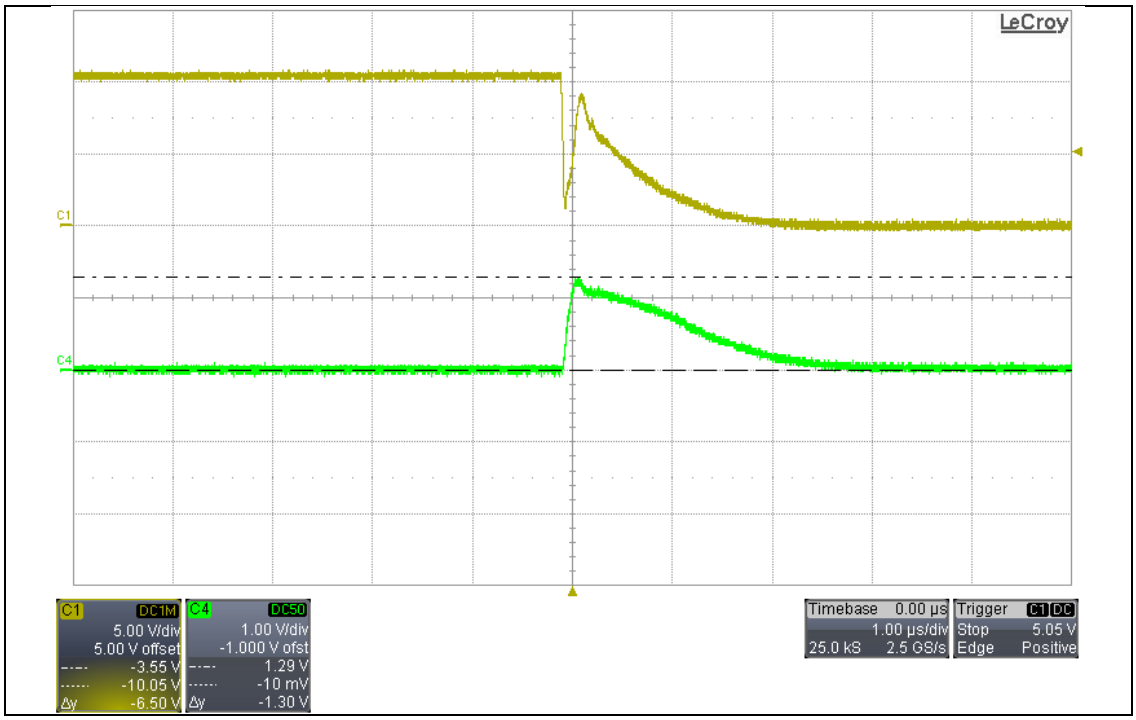
Figure 16. Pre-Driver maximum sourcing current measurement



(1) C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V).

(2) Pre-driver output charging 100nF capacitor. Transient current is measured using Hall current probe showing 1A maximum sourcing capability.

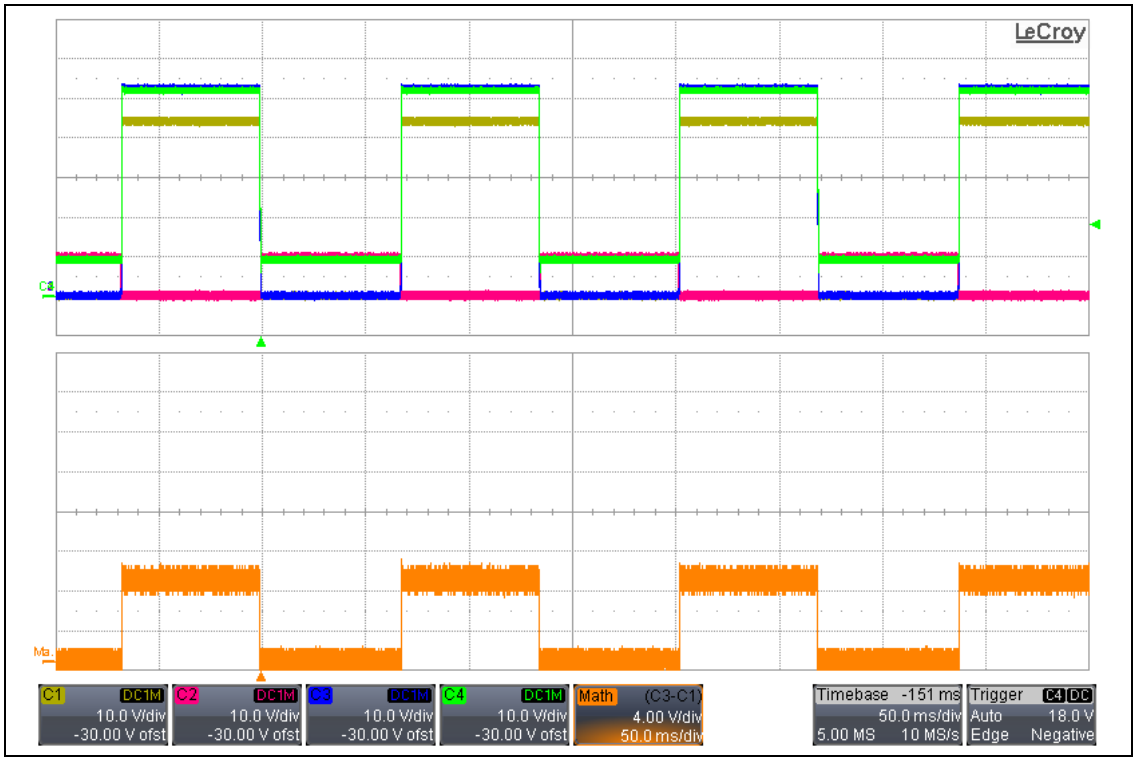
Figure 17. Pre-Driver maximum sinking current measurement



(1) C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V).

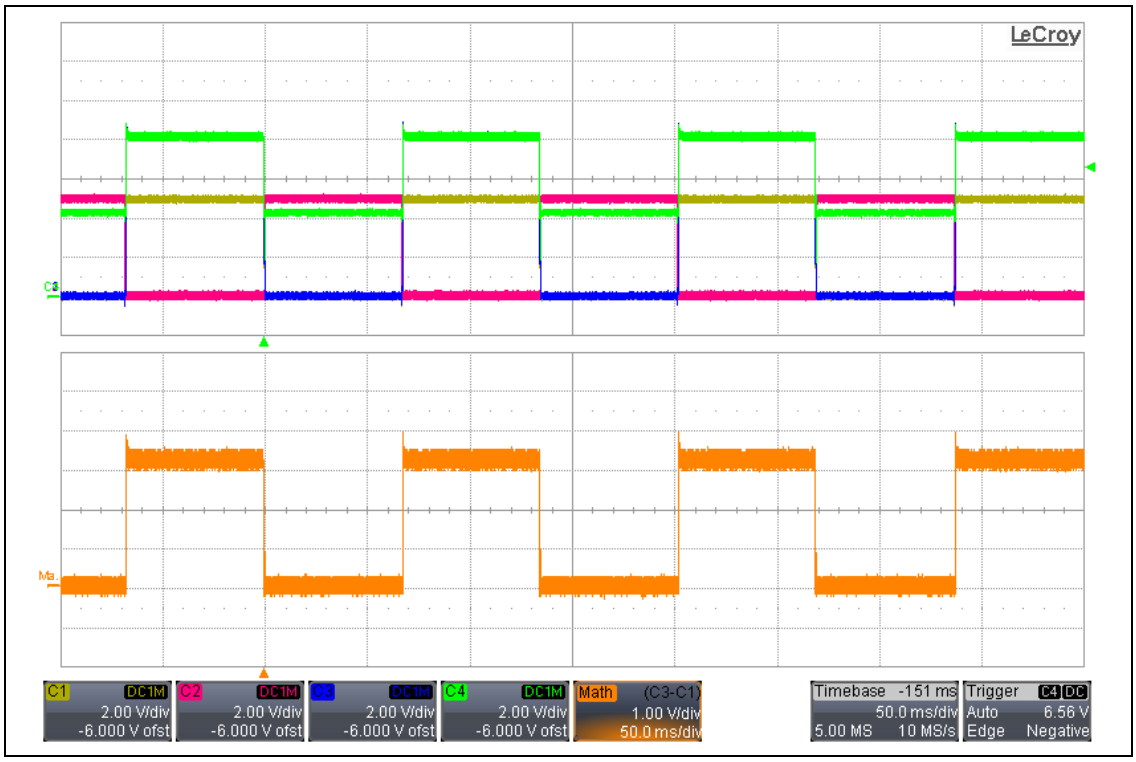
(2) Pre-driver output discharging 100nF capacitor. Transient current is measured using Hall current probe showing 1.3A maximum sinking capability.

Figure 18. Pre-Driver toggling at VBAT=44V



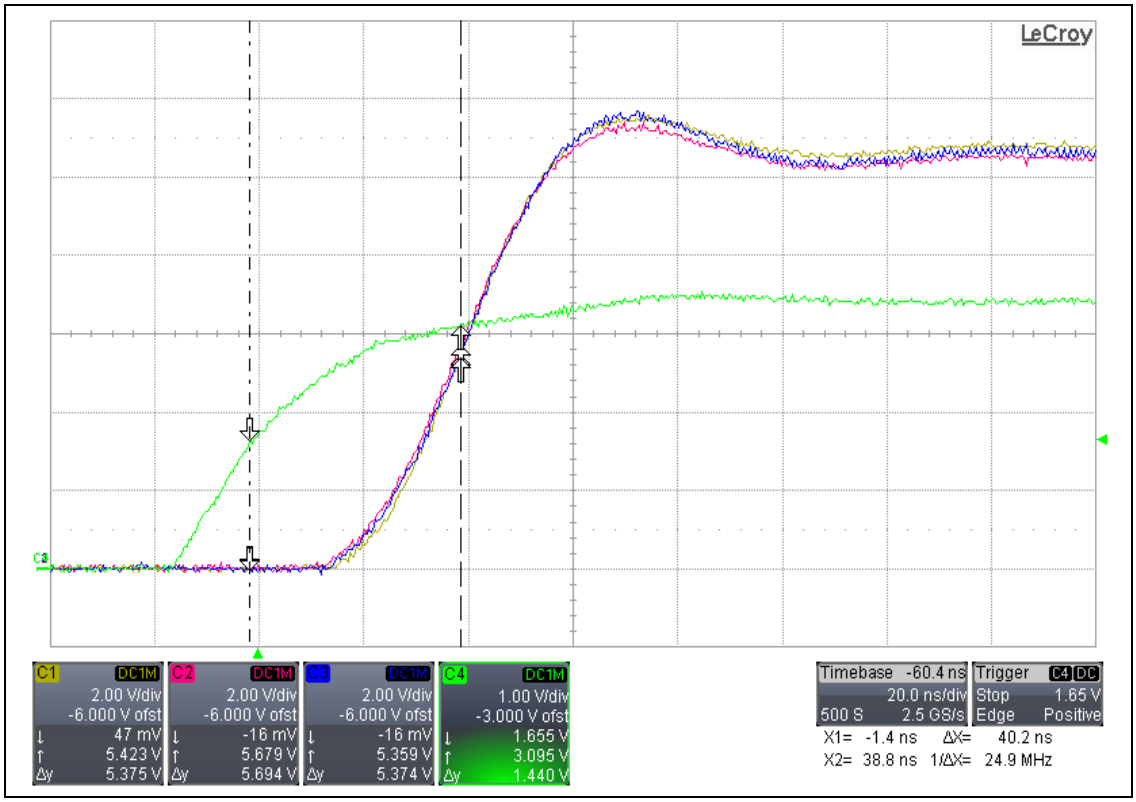
(1) C1 channel – VPX, C2 channel – low-side gate output (OUTL), C3 channel – high-side gate output (OUTH), C4 channel – VBOOT, Math channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 19. Pre-Driver toggling at VBAT=5V



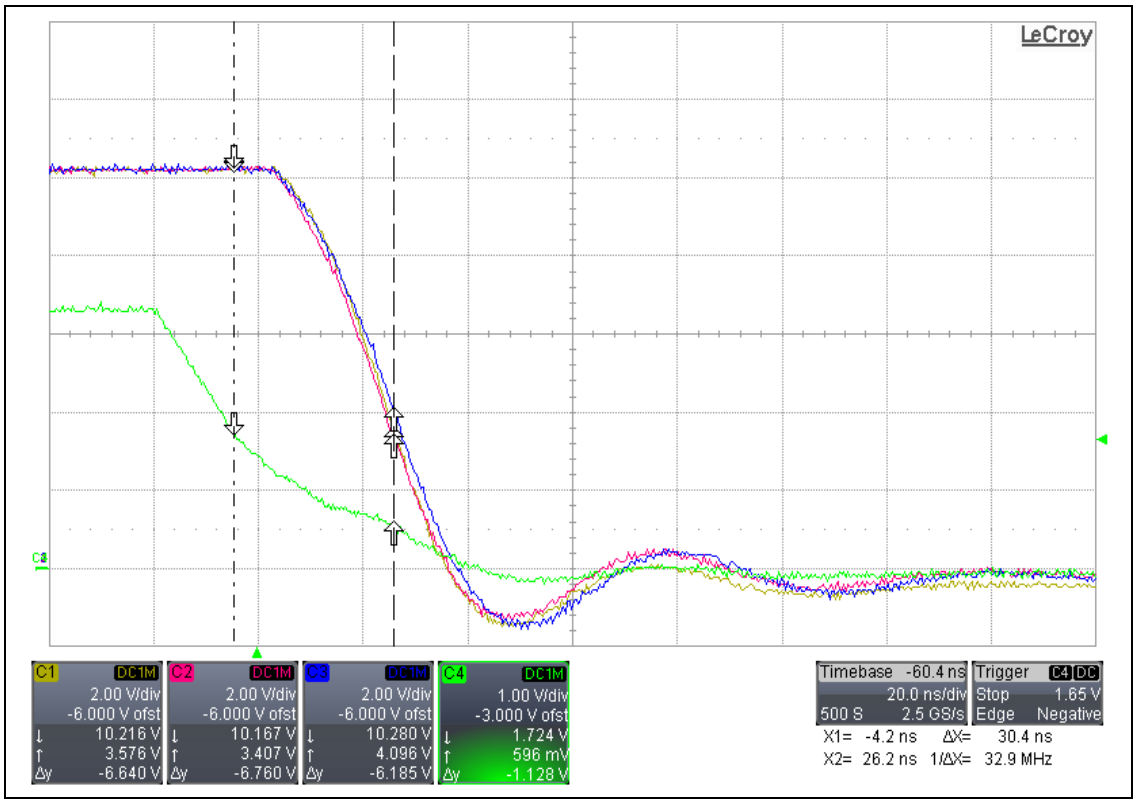
(1) C1 channel – VPX, C2 channel – low-side gate output (OUTL), C3 channel – high-side gate output (OUTH), C4 channel – VBOOT, Math channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 20. Low-side propagation delay measurements (rising edge)



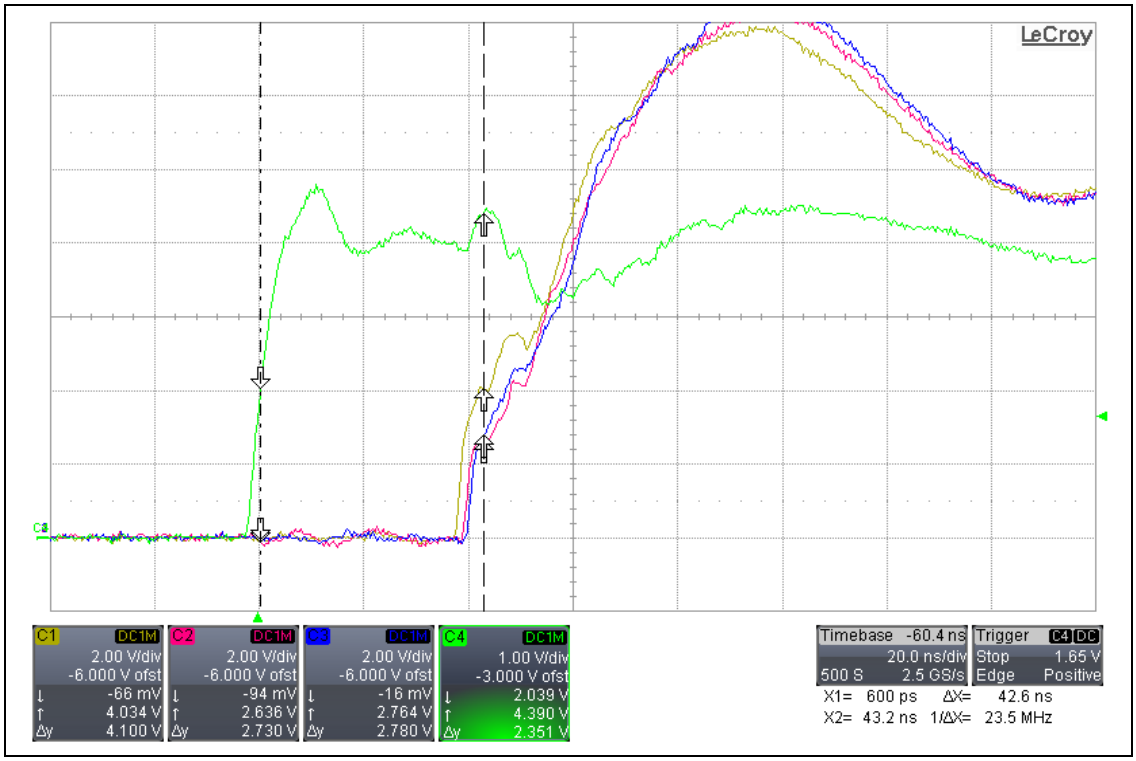
(1) C4 channel – PWM command (broadcasted to each phase); C1/C2/C3 channel – low-side gate outputs for phases U/V/W.

Figure 21. Low-side propagation delay measurements (falling edge)



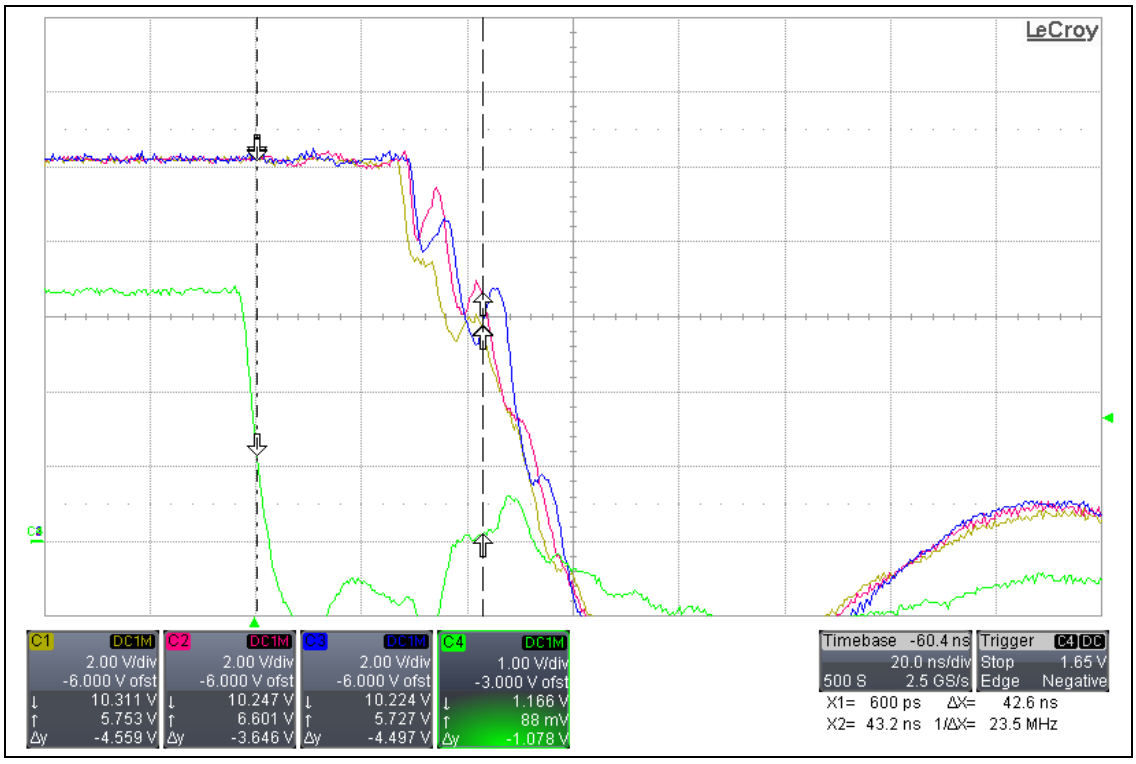
(1) C4 channel – PWM command (broadcasted to each phase); C1/C2/C3 channel – low-side gate outputs for phases U/V/W.

Figure 22. High-side propagation delay measurements (rising edge)



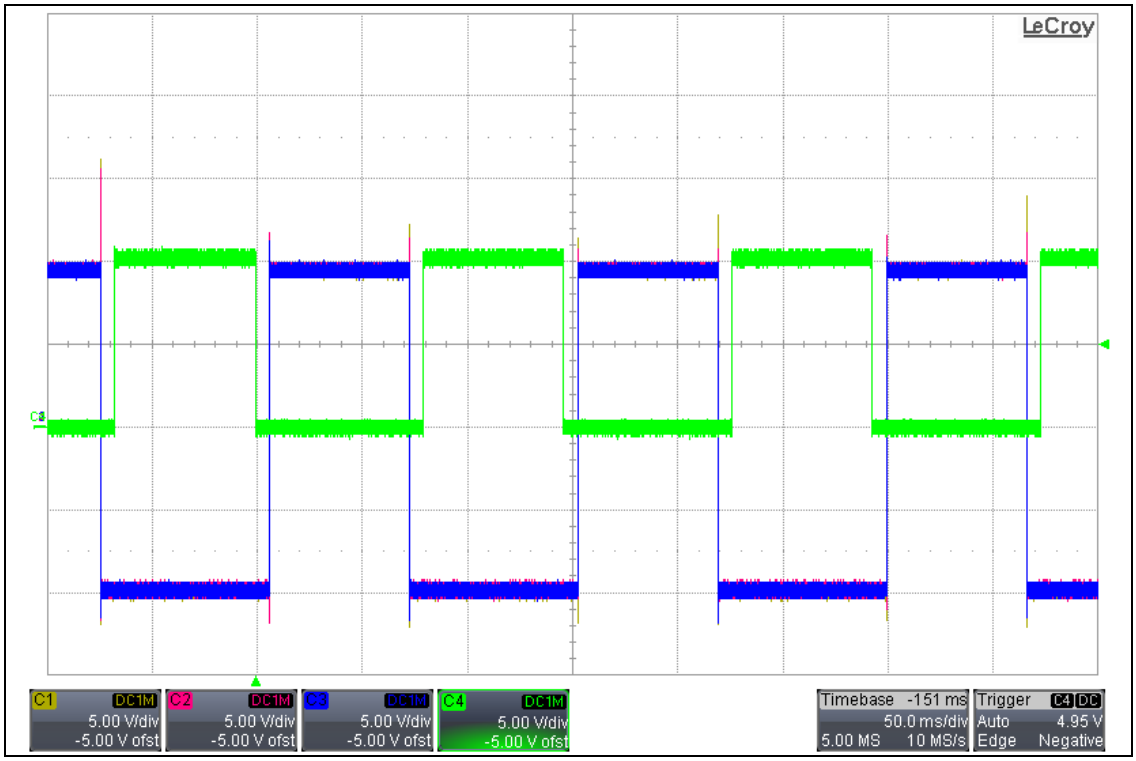
(1) C4 channel – PWM command (broadcasted to each phase); C1/C2/C3 channel – high-side gate outputs for phases U/V/W.

Figure 23. High-side propagation delay measurements (falling edge)



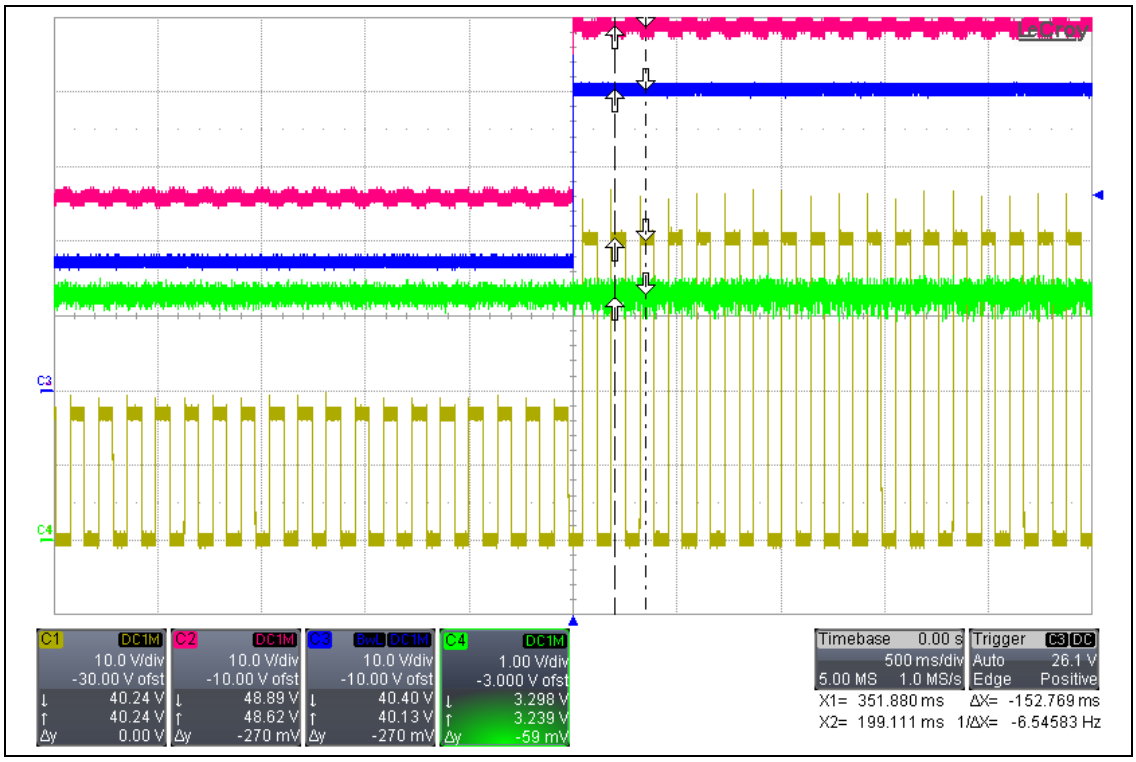
(1) C4 channel – PWM command (broadcasted to each phase); C1/C2/C3 channel – high-side gate outputs for phases U/V/W.

Figure 24. Demonstration of -10V support for all phases toggling in-phase



(1) C1/C2/C3 channel - high-side output for phases U/V/W toggling between -10V and approximately 10V; C4 channel - one of phases' low-side output toggling between 0 and VDDG=10V.

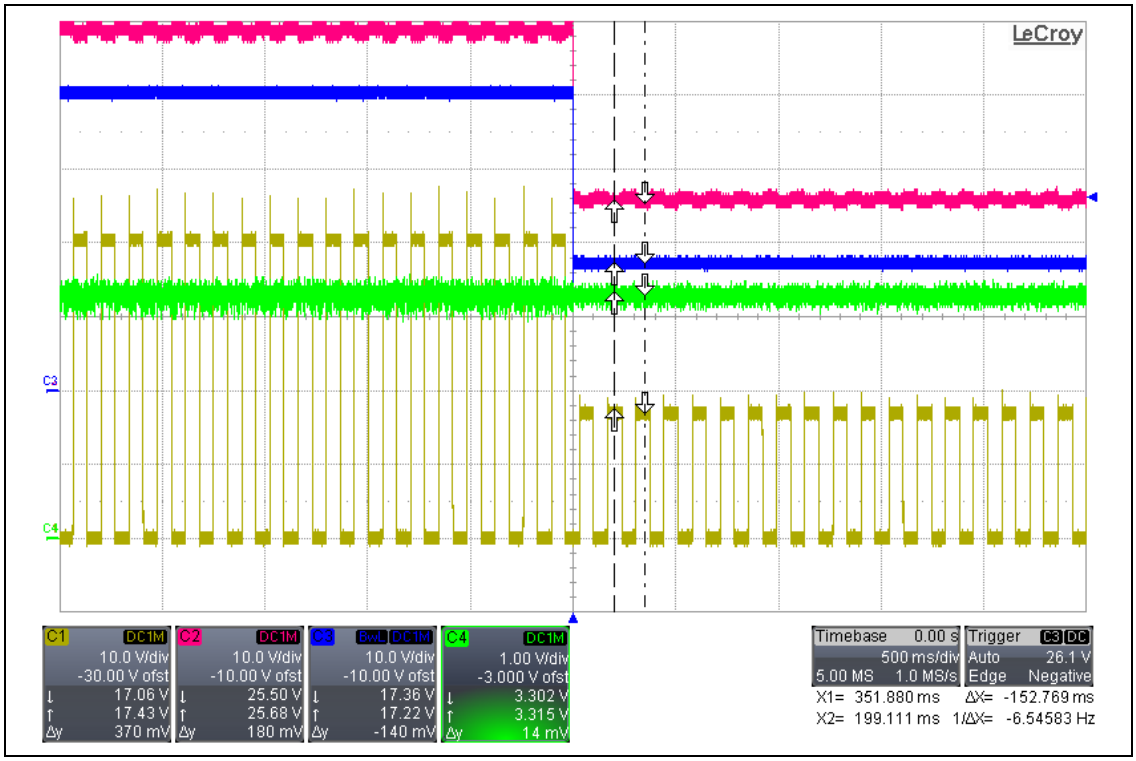
Figure 25. Pre-Driver system response during VBAT power step (from 17V to 40V)



(1) C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.

(2) All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

Figure 26. Pre-Driver system response during VBAT power step (from 40V to 17V)



(1) C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.

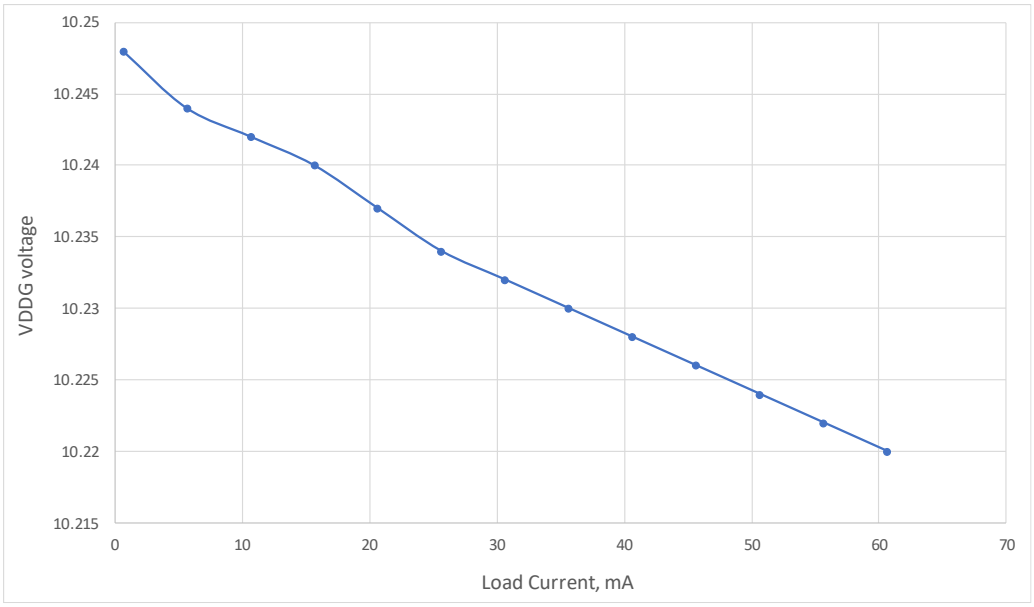
(2) All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

5.21 VDDG LDO characteristics

Table 28. Internal VDDG regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Supply voltage	-	5.5	-	42	V
VDDG	Output voltage	Programmable level	5.5	10	18	V
I_{MAX}	Maximum load current	-	-	-	60	mA

Figure 27. VDDG LDO load regulation for 10V programmable option



5.22 Buck DC-DC regulator characteristics

Table 29. Buck DC-DC regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_Max}	Max recommended operating voltage	-	-	-	42	V
$V_{BAT\_UV\_Trigger}$	Under voltage trigger threshold	-	-	4.15	-	V
$V_{BAT\_UV\_Release}$	Under voltage release threshold	-	-	4.56	-	V
DVDD	3.3V output	-	3.14	3.3	3.47	V
R_{ON_HS}	High side Ron	300mA	-	1.6	-	Ω
R_{ON_LS}	Low side Ron	300mA	-	0.8	-	Ω
I_{Limit}	Valley current limit	-	-	500	-	mA
η	Power efficiency	VBAT = 12V, 170mA, 1.2MHz	-	84	-	%

Figure 28. Buck efficiency for different levels of input power VBAT and current loads

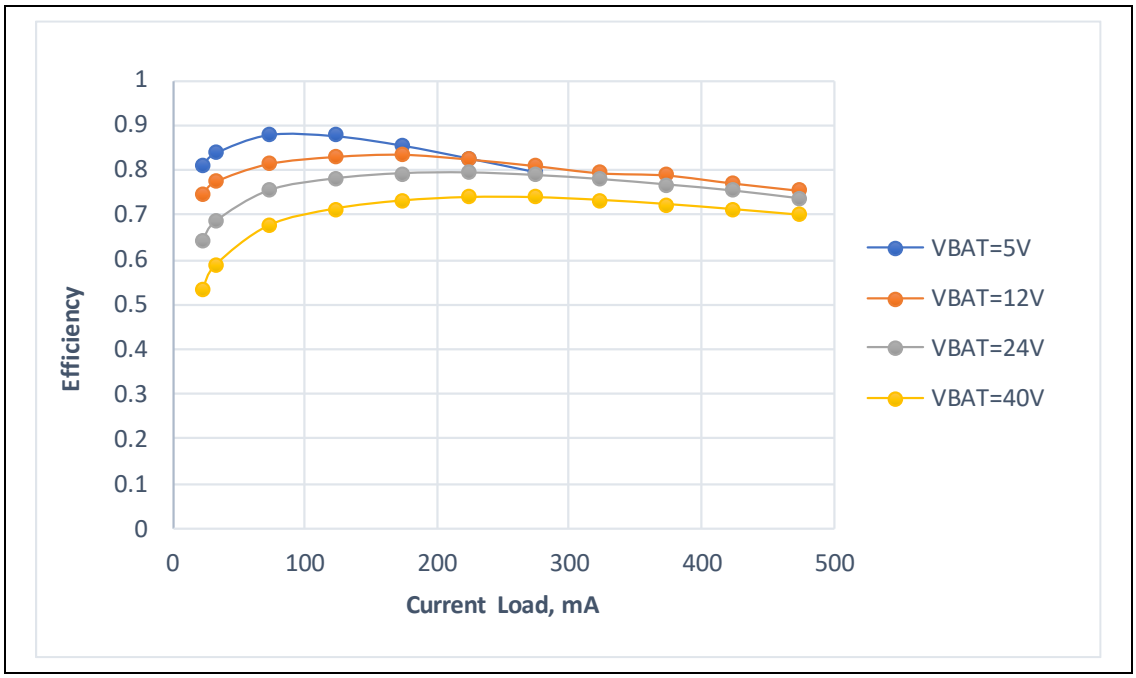
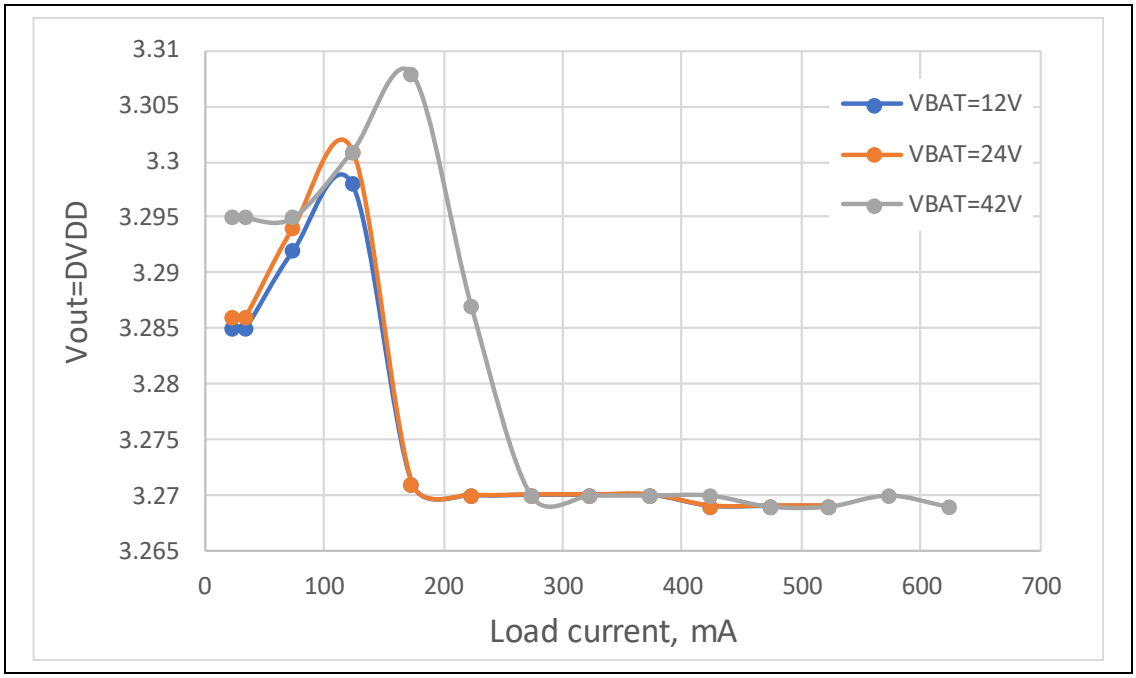


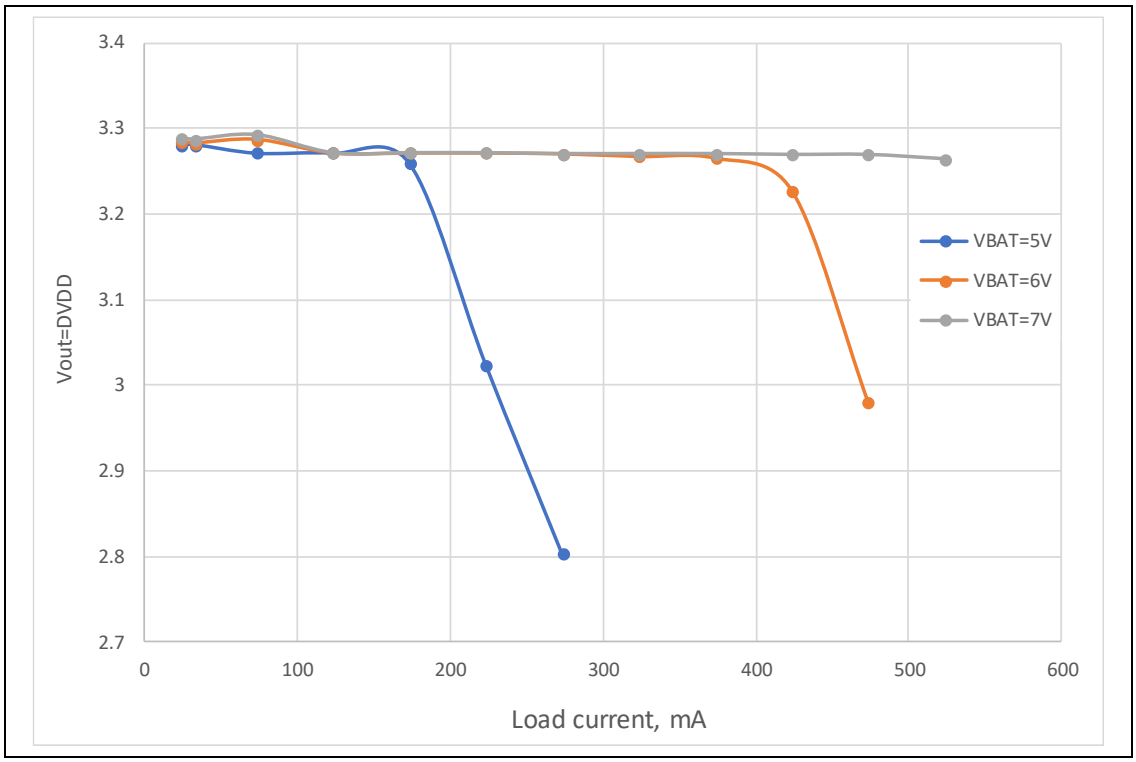
Figure 29. Buck load regulation



(1) Low-current region is in PFM mode and higher-current region transitions to PWM mode.

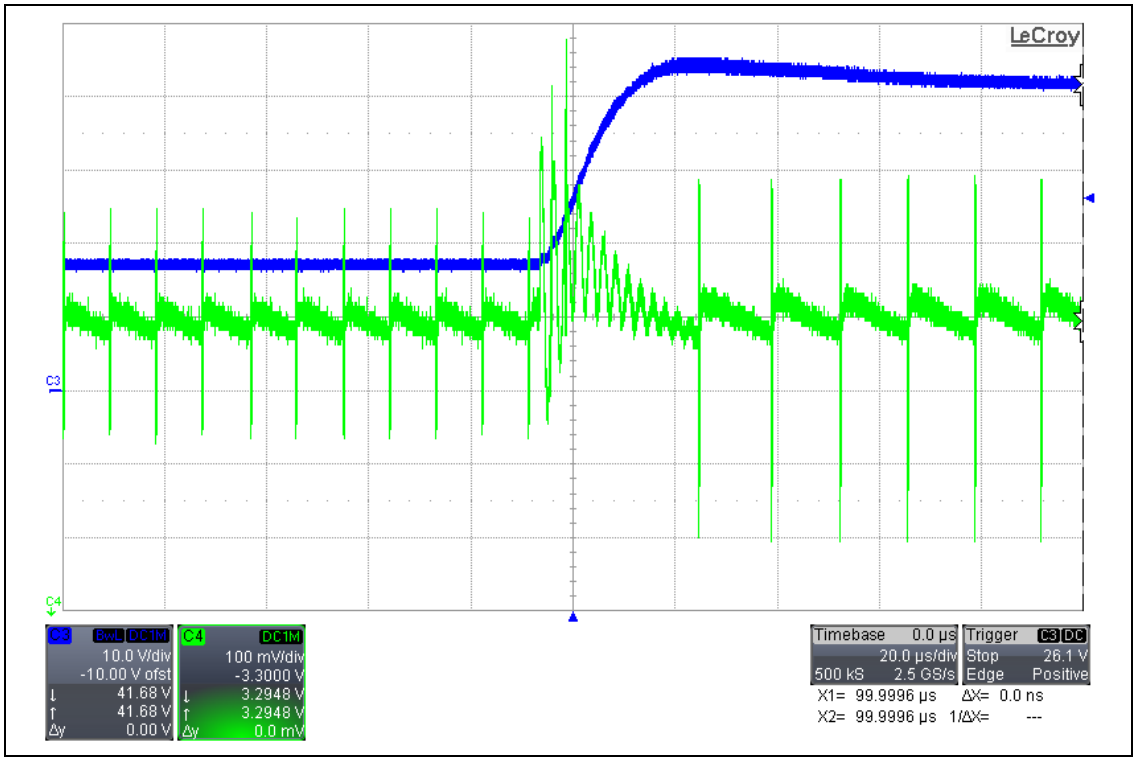
(2) To have a much better load regulation in low-current region, a forced-PWM mode has to be enabled, but at the expense of power efficiency.

Figure 30. Buck load regulation and current capability for low VBAT levels



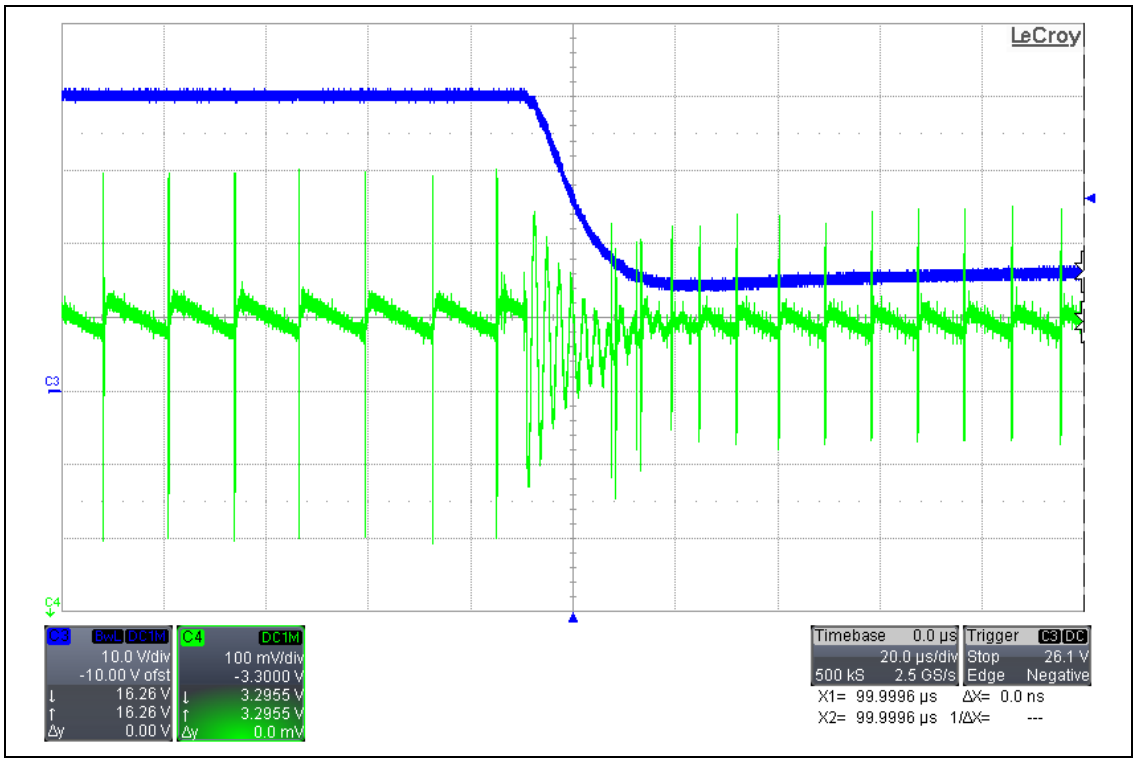
(1) Note that when VBAT< 7V, max current will be affected.

Figure 31. Response of DVDD to VBAT step (from 17V to 40V)



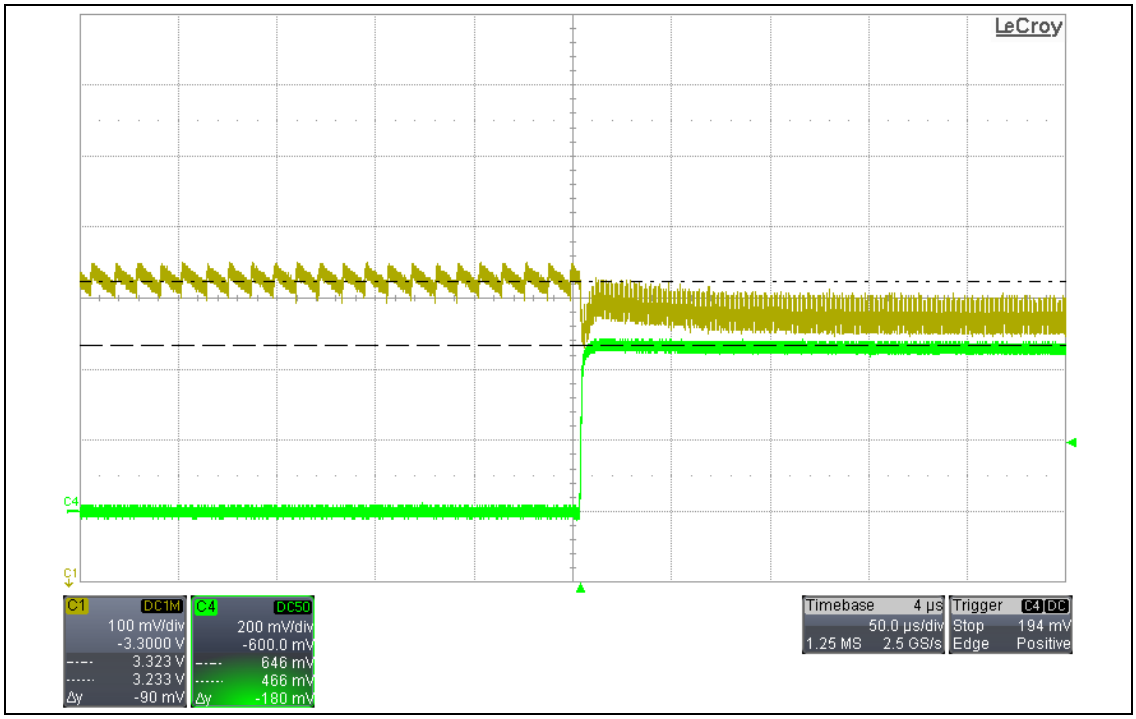
(1) C3 channel – VBAT, C4 channel – DVDD.

Figure 32. Response of DVDD to VBAT step (from 40V to 17V)



(1) C3 channel – VBAT, C4 channel – DVDD.

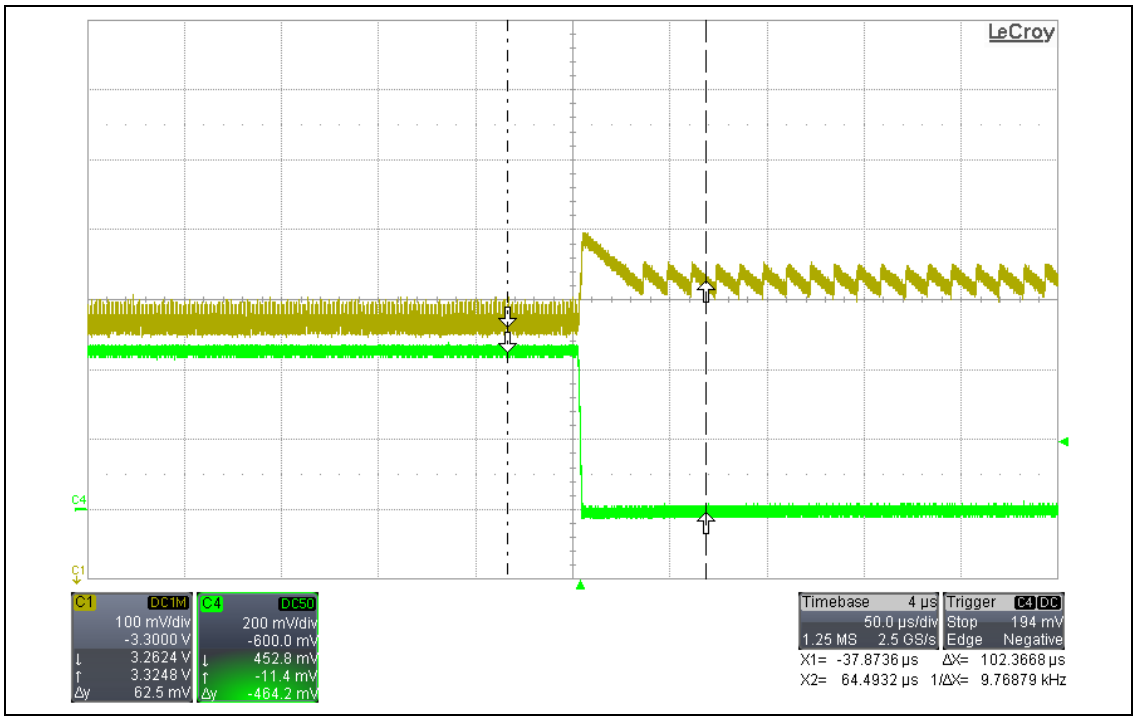
Figure 33. Buck output response to current step at VBAT=24V (from 23mA to 500mA)



(1) C1 channel – DVDD, C4 channel – External current scaled as 1A/1V.

(2) The current of internal chip is counting as 23mA, the overall current switches from 23mA to about 500mA. Buck switches from PFM mode to PWM mode in the step.

Figure 34. Buck output response to current step at VBAT=24V (from 500mA to 23mA)



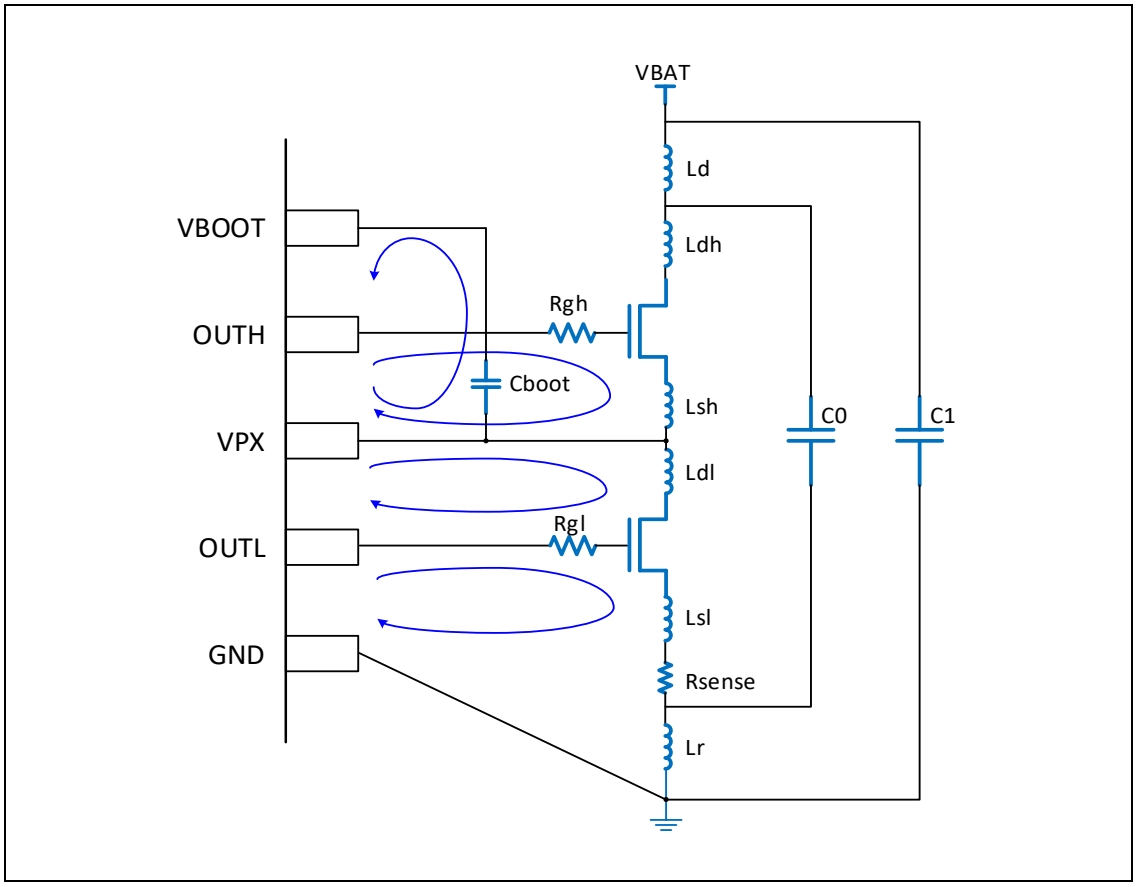
(1) C1 channel – DVDD, C4 channel – External current scaled as 1A/1V.

(2) The current of internal chip is counting as 23mA, the overall current switches from about 500mA to 23mA. Buck switches from PWM mode to PFM mode in the step.

6 PCB layout guidance

- Connect low-ESR bypass capacitors from VBAT, VDDG, DVDD, VDD5, VCAP12 to ground, placing capacitors as close as possible to their respective pins, with the other end of each capacitor having a strong connection to board ground.
- Connect low-ESR capacitor between VCP and VBAT, close to VCP pin.
- Enough through holes should be put under the chip EPAD for a good connection to the copper ground plate. This is essential for thermal dissipation.
- For the Buck DC-DC converter, output capacitor should be put close to the inductor, and the ground connection should be tied to IC ground VSS through short trace or copper plate.
- Co-locate power FET pairs with drain of low-side adjacent to source of high-side to minimize both parasitic Lsh and Ldl. FET pairs should be placed close to each other, in order to reduce routing distance and minimize Lr and Ld (shown in Figure 35).
- Use thick direct tracks between FET's with no loops or wiggling.
- Minimize the areas of major current paths shown by arrows in the diagram of Figure 35 and avoid any loops.
- In case of standing power FET's, reduce the effect of lead inductances by lowering package height above PCB.
- Connect the other end of C0 (shown in Figure 35) as close as possible to the drain of high-side FET, in order to provide the lowest-parasitic return path for current.
- Place IC closer to power switches; route gate driver control signals OUTH and OUTL, and high- and low-side return grounds VPX and GND with straight as-short-as-possible traces.
- Connect bootstrap capacitor as close as possible to VPX and VBOOT pins.
- Use power FET's with fast body diode turn-on times and as small as possible diode reverse charges.
- DVDD is the feedback of buck DCDC, in order to keep the stable operation of control loop, it is recommended to keep DVDD trace away from high voltage switching trace and noisy source, such as inductor, etc.
- Keep the switching trace as short and wide as practical in order to minimize radiated emissions.
- The GND trace between the DVDD capacitor and the GND pin should be as wide as possible so that trace impedance is minimized.

Figure 35. Simplified Pre-Driver Board Diagram

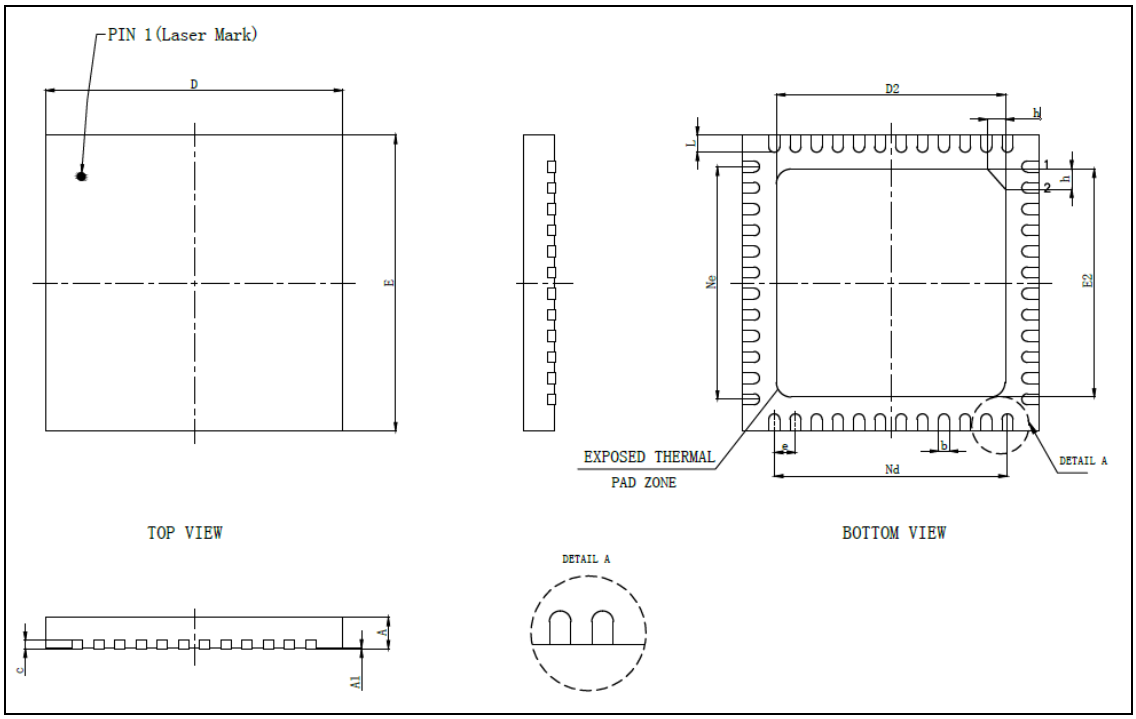


7 Package information

The package type of SPD1148 is 48-pin or 60-pin QFN. The detail information is as follows:

7.1 QFN48

Figure 36. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead package outline

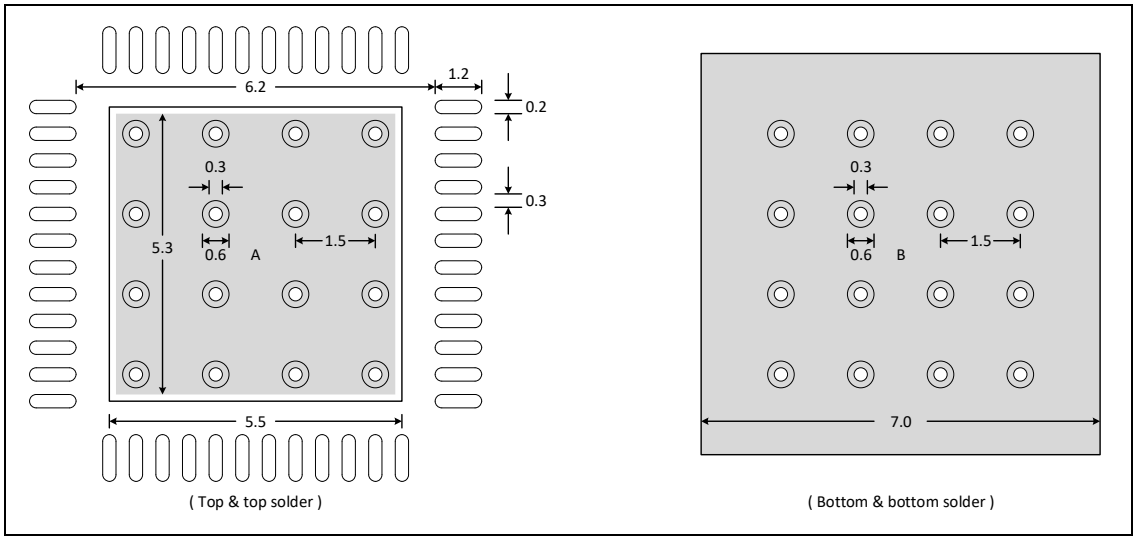


(1) Drawing is not to scale.

Table 30. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.23
D	6.90	7.00	7.1
D2	5.30	5.40	5.50
e	0.50		
Ne	5.50		
Nd	5.50		
E	6.90	7.00	7.10
E2	5.30	5.40	5.50
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 37. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead recommended footprint

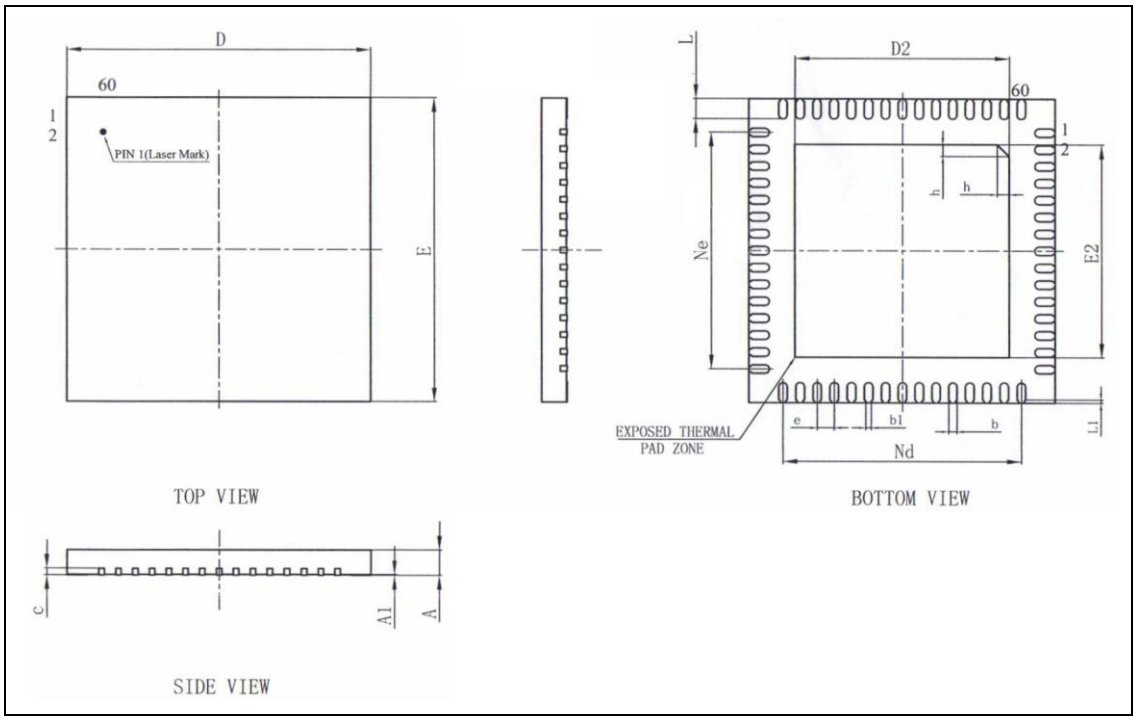


(1) Dimensions are expressed in millimeters.

(2) The A area on the top layer should brush solder paste, and B area on bottom layer can either brush solder paste or not.

7.2 QFN60

Figure 38. QFN60 – 60 pin, 9mm x 9mm quad flat no-lead package outline



(2) Drawing is not to scale.

Table 31. QFN60 – 60 pin, 9mm x 9mm quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.16	
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	6.20	6.30	6.40
e		0.50	
Ne		7.00	
Nd		7.00	
E	8.90	9.00	9.10
E2	6.20	6.30	6.40
L	0.50	0.60	0.70
L1		0.10	
h	0.30	0.35	0.40

8 Ordering information

Table 32. Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package	Temperature Range	SPQ(1)	Packing
SPD1148API48	128KB	64KB	200MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148ZAPI48	64KB	32KB	200MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148YAPI48	32KB	16KB	200MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148XAPI48	128KB	64KB	100MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148WAPI48	64KB	32KB	100MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148VAPI48	32KB	16KB	100MHz	QFN48	Industrial -40 °C to +125 °C	2600	Tray
SPD1148API60	128KB	64KB	200MHz	QFN60	Industrial -40 °C to +125 °C	2600	Tray

(1) SPQ = Standard Pack Quantity.

9 Revision history

Table 33. Document revision history

Date	Revision	Changes
08-Oct-2019	1	Initial release.
20-Dec-2019	2	1. Add Table 22. ESD absolute maximum ratings. 2. Add Table 23. Electrical sensitivities.
05-Mar-2020	3	1. Update Section 2.8, add safety clock description. 2. Update Section 2.9 for boot mode description.
03-Apr-2020	4	1. Update Table 5. Absolute maximum ratings (1)(2). 2. Update Table 29. Buck DC-DC regulator characteristics.
13-Jun-2020	5	1. Update Section 2.9 for boot mode description. 2. Update Section 2.14 and modify the maximum speed of SPI. 3. Update Section 2.18 for phase comparison. 4. Update Table 7. I/O Electrical characteristics. 5. Update Table 11. Internal 1.2V regulator characteristics. 6. Update Figure 9. Internal 1.2V regulator load regulation. 7. Add Table 12. BOD characteristics. 8. Add Table 13. RCO characteristics. 9. Add Table 14. PLL characteristics. 10. Add Table 15. XO characteristics. 11. Update Table 16. ADC characteristics. 12. Add Chapter 8 for ordering information. 13. Add Table 26. SPI characteristics. 14. Add Figure 16. Pre-Driver maximum sourcing current measurement. 15. Add Figure 17. Pre-Driver maximum sinking current measurement. 16. Add Figure 18. Pre-Driver toggling at VBAT=44V. 17. Add Figure 19. Pre-Driver toggling at VBAT=5V. 18. Add Figure 20. Low-side propagation delay measurements (rising edge). 19. Add Figure 21. Low-side propagation delay measurements (falling edge). 20. Add Figure 22. High-side propagation delay measurements (rising edge). 21. Add Figure 23. High-side propagation delay measurements (falling edge). 22. Add Figure 24. Demonstration of -10V support for all phases toggling in-phase. 23. Add Figure 25. Pre-Driver system response during VBAT power step (from 17V to 40V). 24. Add Figure 26. Pre-Driver system response during VBAT power step (from 40V to 17V).

Date	Revision	Changes
		25. Add Table 28. Internal VDDG regulator characteristics. 26. Add Figure 27. VDDG LDO load regulation for 10V programmable option. 27. Add Figure 28. Buck efficiency for different levels of input power VBAT and current loads. 28. Add Figure 29. Buck load regulation. 29. Add Figure 30. Buck load regulation and current capability for low VBAT levels. 30. Add Figure 31. Response of DVDD to VBAT step (from 17V to 40V). 31. Add Figure 32. Response of DVDD to VBAT step (from 40V to 17V). 32. Add Figure 33. Buck output response to current step at VBAT=24V (from 23mA to 500mA). 33. Add Figure 34. Buck output response to current step at VBAT=24V (from 500mA to 23mA).
31-Jul-2020	6	1. Update Section 2.12 for UART features. 2. Add Figure 10. Internal 1.2V regulator load regulation with different temperature. 3. Update Table 17. PGA characteristics. 4. Update Table 21. Flash memory characteristics.
28-Mar-2021	7	1. Update Table 7. I/O Electrical characteristics. 2. Update Table 8. SPD1148 typical current consumption (Run in FLASH). 3. Update Table 9. SPD1148 typical current consumption (Run in RAM). 4. Update Figure 7. Typical operational current versus frequency. 5. Update VBAT minimum value with 5V. 6. Add characteristics of ambient temperature T_A. 7. Update Table 32. Ordering information. 8. Update Section 2.12 for UART features. 9. Update Table 17. PGA characteristics. 10. Add Figure 37. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead recommended footprint. 11. Add Table 3. PGA input channel selection. 12. Update comparator pin descriptions in Table 1. 13. Add Table 4. GPIO pin function and state after reset. 14. Add note for Table 8. SPD1148 typical current consumption (Run in FLASH). 15. Add note for Table 9. SPD1148 typical current consumption (Run in RAM). 16. Update Table 10. Peripheral current consumption. 17. Add Table 25. Thermal resistance characteristics (QFN48 package). 18. Update Figure 4. SPD1148 QFN48 pin-out and its notes.
26-Nov-2021	8	1. Add Table 24. Moisture sensitivity characteristic. 2. Update Table 3. PGA input channel selection.

Date	Revision	Changes
		3. Update Figure 37. QFN48 – 48 pin, 7mm x 7mm quad flat no-lead recommended footprint. 4. Update Table 5. Absolute maximum ratings (1)(2). 5. Update Table 18. Comparator characteristics. 6. Add Figure 11. The negative resistance of the on-chip crystal oscillator at 50℃. 7. Add Figure 12. The negative resistance of the on-chip crystal oscillator at 85℃. 8. Add Figure 13. The negative resistance of the on-chip crystal oscillator at 100℃. 9. Add Figure 14. The negative resistance of the on-chip crystal oscillator at 125℃. 10. Update Table 1. SPD1148 QFN48 pin definitions, modify the description for debug pins.
08-Jul-2022	9	1. Update Section 2.21. 2. Update Table 7. I/O Electrical characteristics, remove parameter I_{OZ}. 3. Update Chapter 6. 4. Add Pin and package information for QFN60. 5. Update Section 2.9 and Section 2.10. 6. Update Conditions of parameter R_{PU} and R_{PD} in Table 7. I/O Electrical characteristics. 7. Update Table 3. PGA input channel selection. 8. Update the minimum operating VBAT voltage from 5V to 5.5V. 9. Update Table 1. SPD1148 QFN48 pin definitions.
09-Aug-2022	10	1. Update the minimum operating VBAT voltage from 5V to 5.5V. 2. Update Table 1. SPD1148 QFN48 pin definitions, fix the document error that PIN 26 is written as 28.
14-Sep-2022	11	1. Update Table 32. Ordering information, change ordering number. 2. Update the minimum supply voltage from 5V to 5.5V in Section 2.6.