Application note

UART protocol used in the SPD1179 IAP loader

Revision 1 – October 2021

Introduction

This application note describes the UART protocol used in the SPD1179 IAP loader. It details each supported command and the sequences to download user application code.

Contents

List of tables

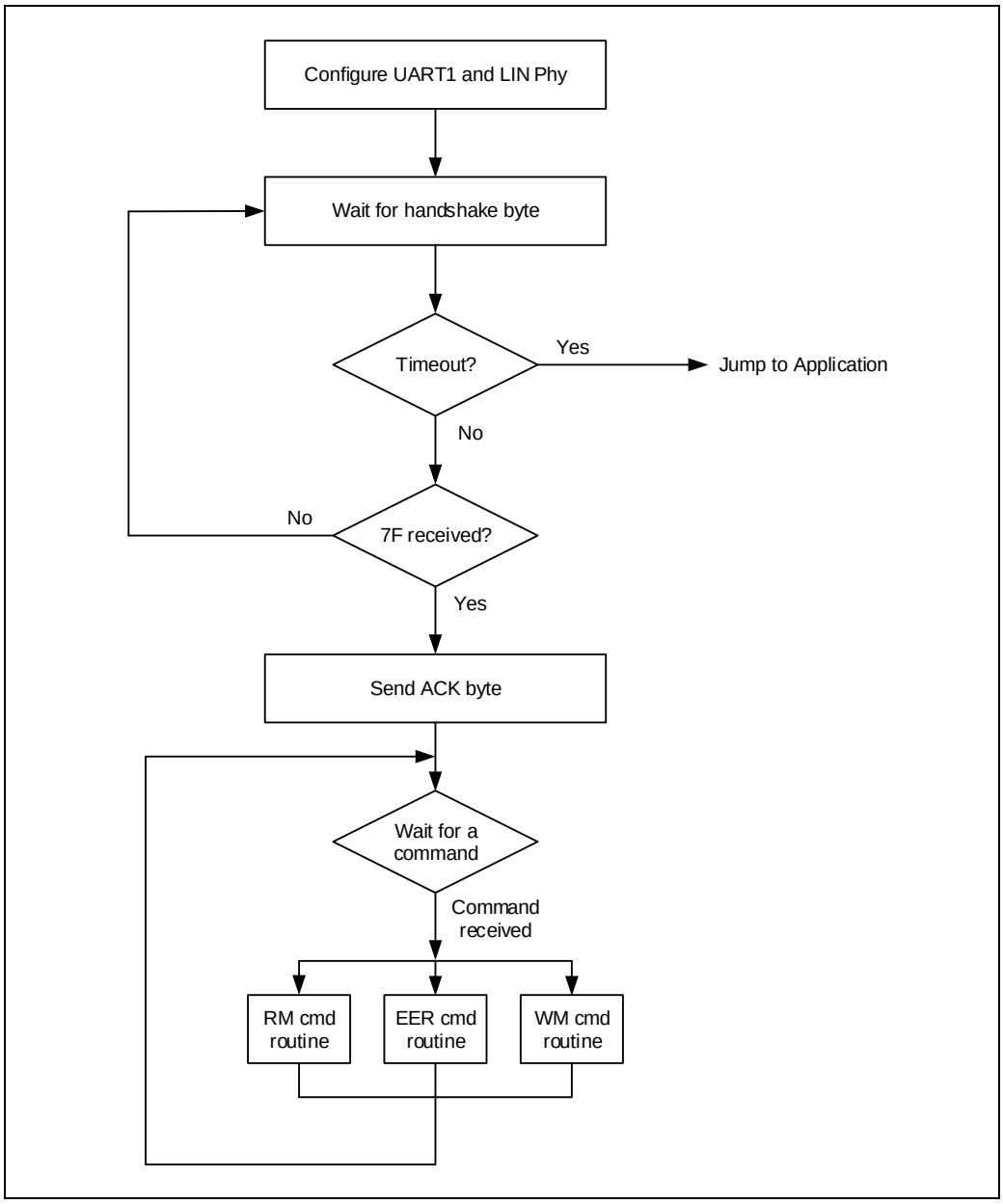
List of figures

1 IAP loader sequence

Once the SPD1179 microcontroller has been configured, the IAP loader begins to wait to receive the 0x7F data frame: one start bit, eight data bits, none parity and one stop bit. Then an acknowledge byte (0x79) is returned to the host, which means that the SPD1179 is successful to handshake with the host.

Figure 1 shows the IAP loader sequence for SPD1179.

Figure 1. IAP loader sequence for SPD1179



2 IAP loader command set

The supported commands are listed in *Table 1* below. Each command is further described in this section.

Table 1. IAP loader commands

Command	Command code	Command description
Read Memory	0x11	Reads up to 256 bytes of memory starting from an address specified by the application
Write Memory	0x31	Writes up to 256 bytes to the Flash memory starting from an address specified by the application
Extended Erase	0x44	Erases from one to all the Flash memory pages using two byte addressing mode

Communication safety

All communications from the programming tool to the device are verified by:

1. Checksum: received blocks of data bytes are XORed. A byte containing the computed XOR of all previous byte is added to the end of each communication (checksum byte). By XORing all received bytes, data + checksum, the result at the end of the packet must be 0x00.
2. For each command the host sends a byte and its complement (XOR = 0x00).

Note: XOR (A, B) = 0xFF^A^B

Each packet is either accepted (ACK answer) or discarded (NACK answer):

- ACK = 0x79
- NACK = 0x1F

2.1 Read Memory command

The Read Memory command is used to read data from any valid memory address in Flash memory.

When the IAP loader receives the Read Memory command, it transmits the ACK byte to the application. After the transmission of the ACK byte, the IAP loader waits for an address (4 bytes, byte 1 is the address LSB and byte 4 is the MSB), the number of bytes to be transmitted – 1 (N bytes) and a checksum byte, then it checks the checksum and the received address. If the address is valid and the checksum is correct, the IAP loader transmits an ACK byte and the needed data ((N + 1) bytes, starting from the received address) to the application, otherwise it transmits a NACK byte and aborts the command.

The host sends bytes to the SPD1179 as follows:

Bytes 1-2: 0x11+0xEE
Wait for ACK

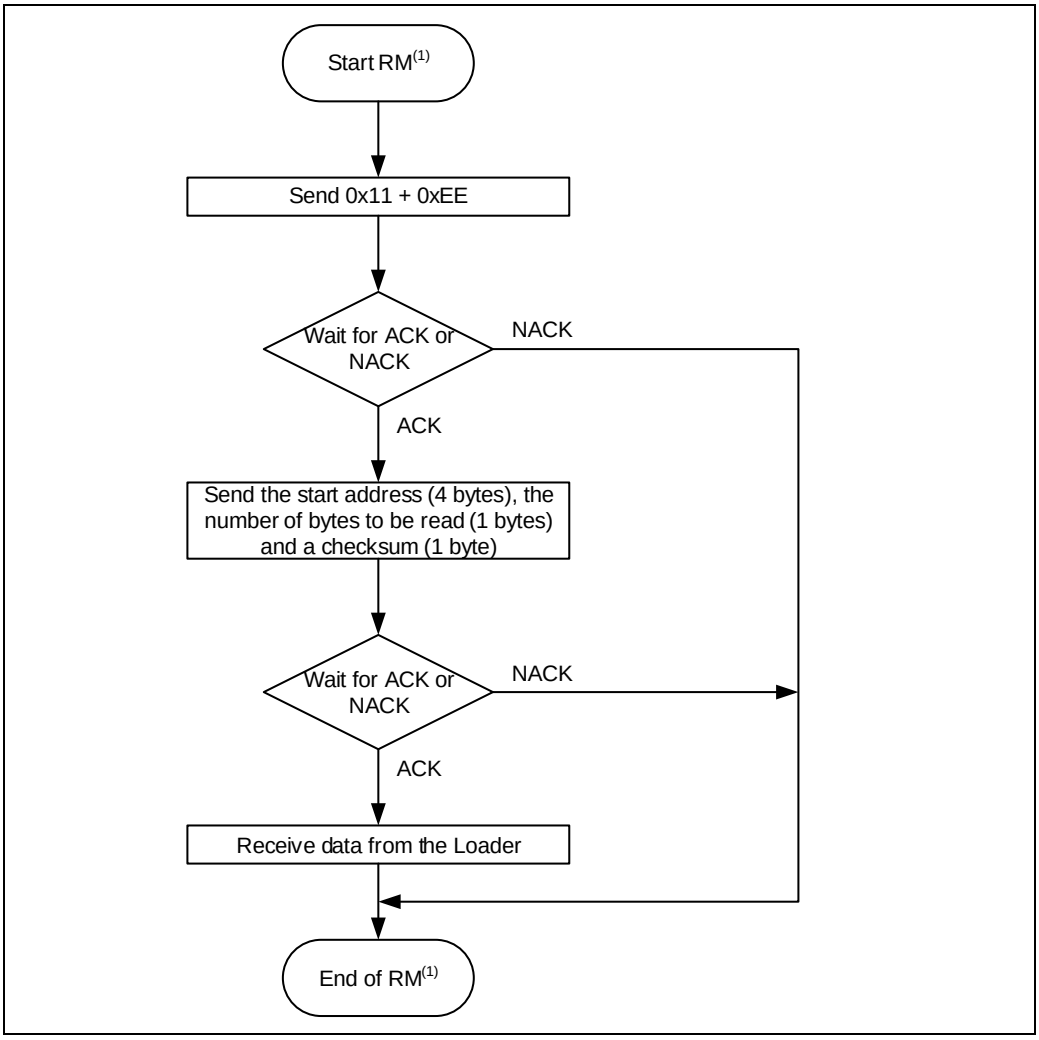
Bytes 3 to 6: Start address

- byte 3: LSB
- byte 6: MSB

Byte 7: The number of bytes to be read - 1 ($0 < N \leq 255$)

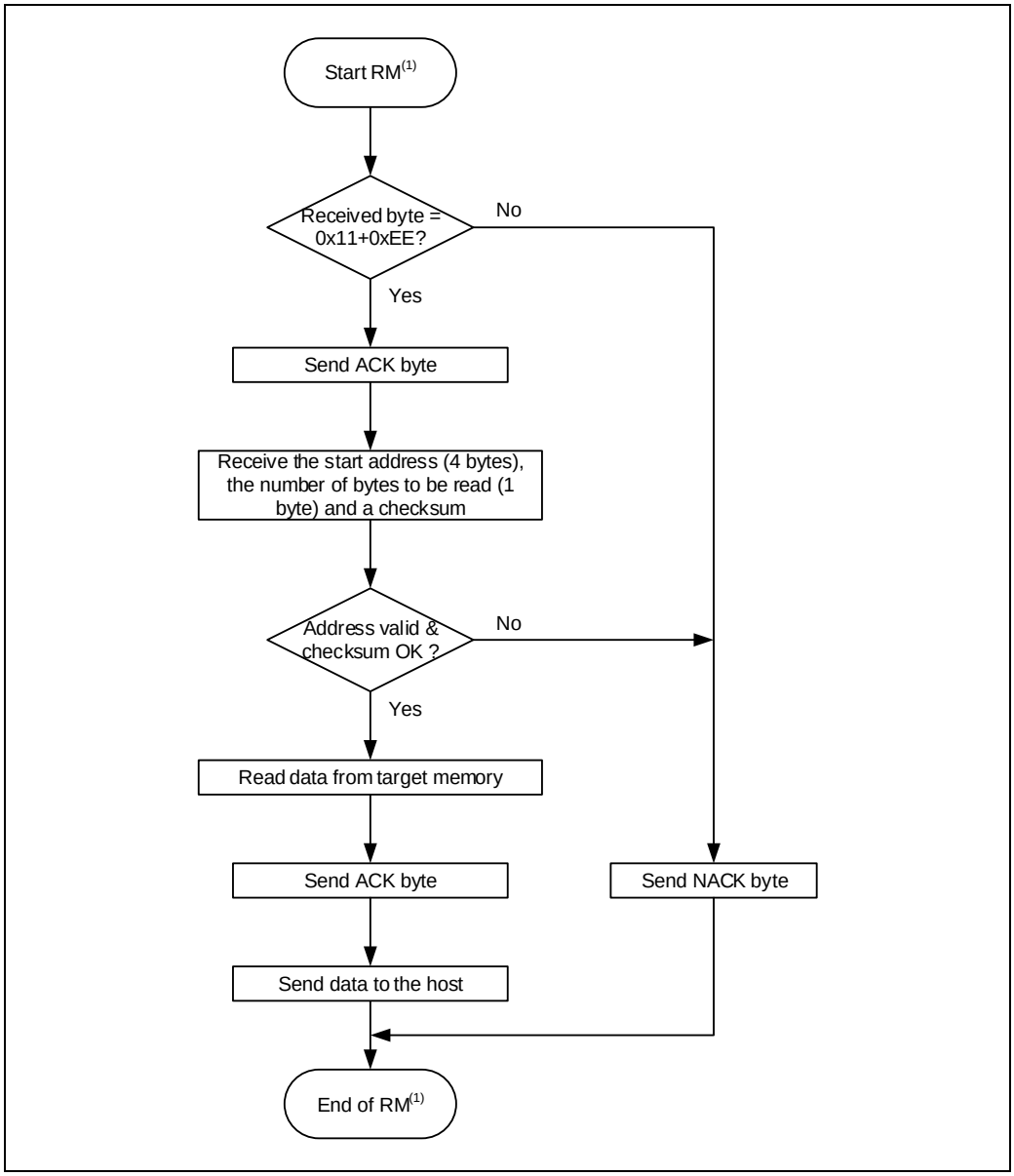
Byte 8: Checksum: XOR (byte 3, byte 4, byte 5, byte 6, byte 7)
Wait for ACK

Figure 2. Read Memory command: host side



1. RM = Read Memory.

Figure 3. Read Memory command: device side



1. RM = Read Memory.

2.2 Write Memory command

The Write Memory command is used to write data to any valid memory address, i.e. Flash memory.

When the IAP loader receives the Write Memory command, it transmits the ACK byte to the application. After the transmission of the ACK byte, the IAP loader waits for an address (4 bytes, byte 1 is the address LSB and byte 4 is the MSB) and a checksum byte, it then checks the received address. If the received address is valid and the checksum is correct, the IAP loader transmits an ACK byte, otherwise it transmits a NACK byte and aborts the command. When the address is valid and the checksum is correct, the IAP loader:

- gets a byte, N, which contains the number of data bytes to be received

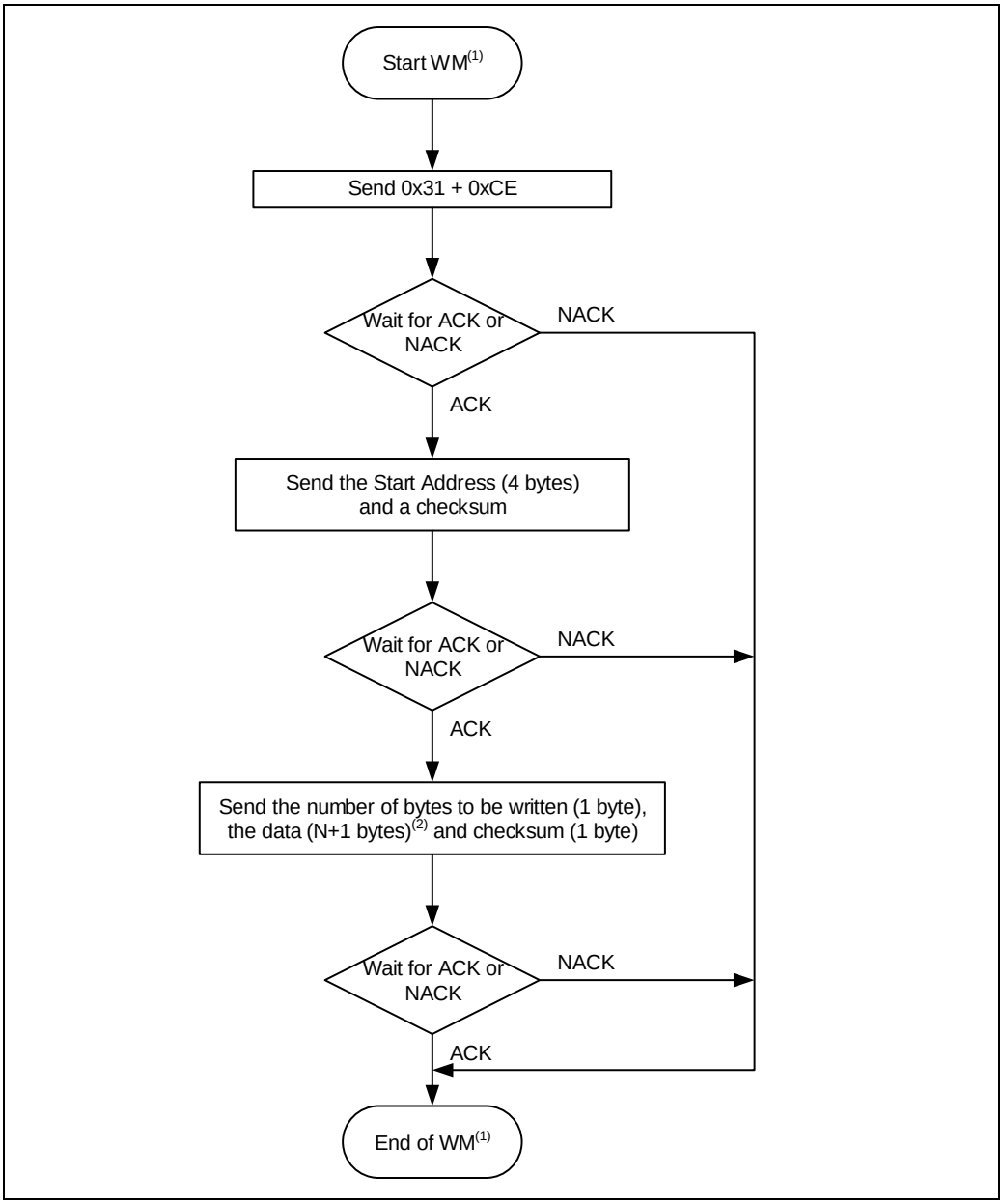
- receives the user data ((N + 1) bytes) and the checksum (XOR of N and of all data bytes)
- programs the user data to memory starting from the received address
- at the end of the command, if the write operation was successful, the IAP loader transmits the ACK byte; otherwise it transmits a NACK byte to the application and aborts the command

The maximum length of the block to be written for the SPD1179 is 256 bytes.

The host sends bytes to the SPD1179 as follows:

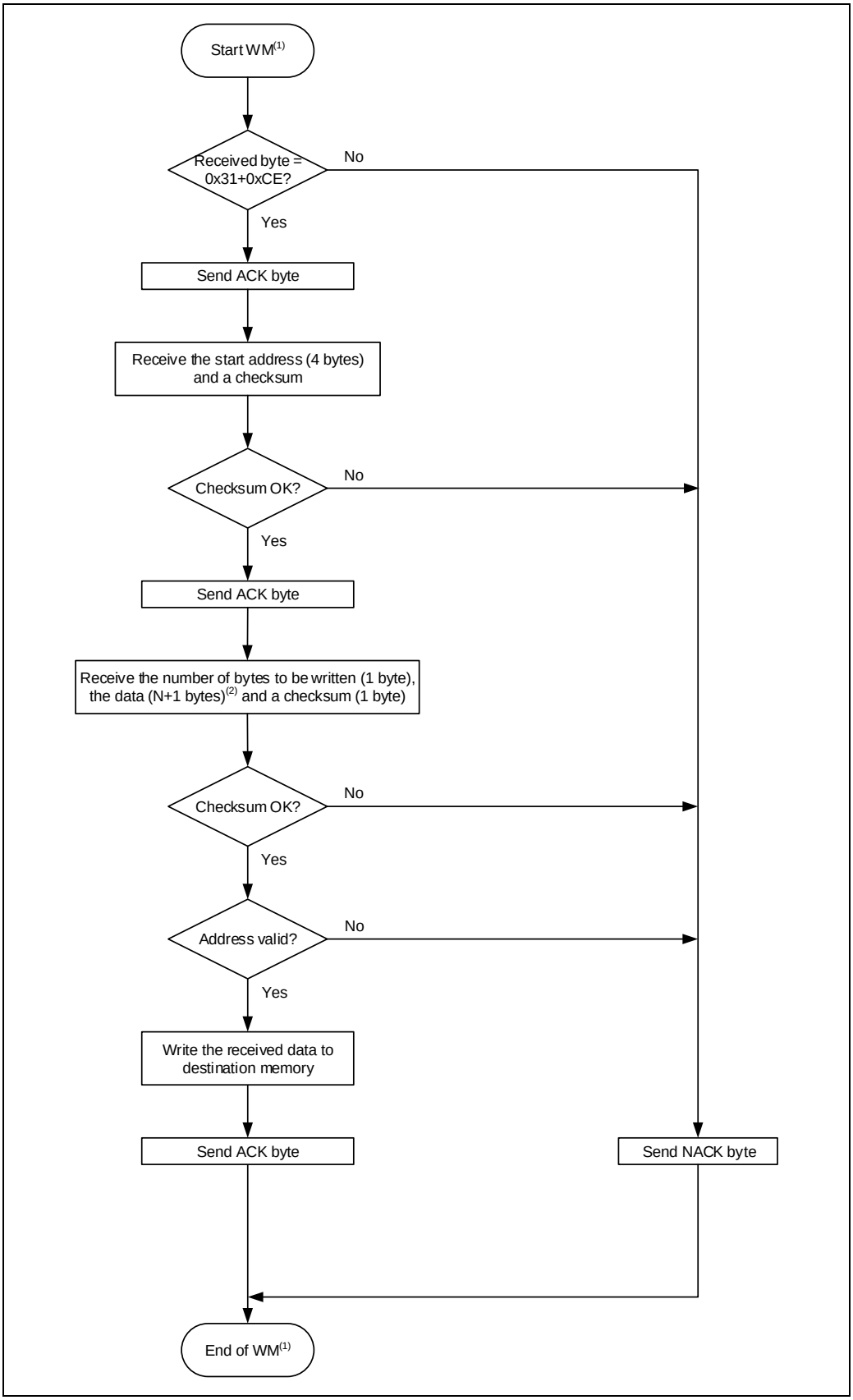
Byte 1:	0x31
Byte 2:	0xCE
	Wait for ACK
Byte 3 to 6:	Start address • byte 3: LSB • byte 6: MSB
Byte 7:	Checksum: XOR (Byte3, Byte4, Byte5, Byte6)
	Wait for ACK
Byte 8:	Number of bytes to be written (0 < N ≤ 255)
N +1 data bytes:	(Max 256 bytes)
Checksum byte:	XOR (N, N+1 data bytes)

Figure 4. Write Memory command: host side



1. WM = Write Memory.
2. N+1 should always be a multiple of 4.

Figure 5. Write Memory command: device side



1. WM = Write Memory.
2. N+1 should always be a multiple of 4.

2.3 Extended Erase Memory command

The Extended Erase Memory command allows the host to erase Flash memory pages using two bytes addressing mode. When the IAP loader receives the Extended Erase Memory command, it transmits the ACK byte to the host. After the transmission of the ACK byte, the IAP loader receives two bytes (number of pages to be erased), the Flash memory page codes (each one coded on two bytes, LSB first) and a checksum byte (XOR of the sent bytes); if the checksum is correct, the IAP loader erases the memory and sends an ACK byte to the host. Otherwise it sends a NACK byte to the host and the command is aborted.

Extended Erase Memory command specifications:

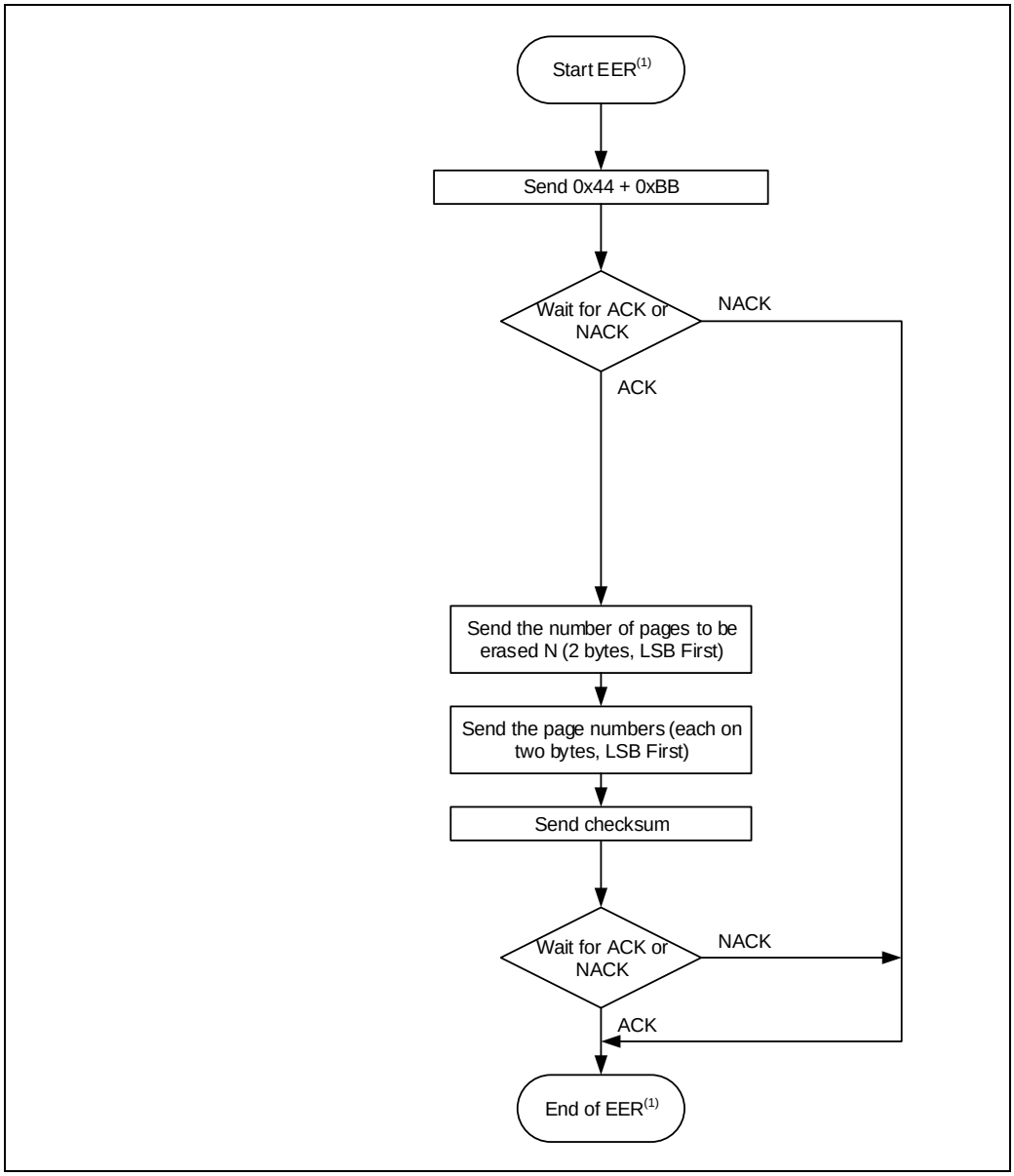
1. The IAP loader receives one half-word (two bytes) that contain N, the number of pages to be erased:
   a) For values where 0 ≤ N < maximum number of pages: N + 1 pages are erased.

2. The IAP loader receives:
   a) In the case of N+1 page erase, the IAP loader receives (2 x (N + 1)) bytes, each half-word containing a page number (coded on two bytes, LSB first). Then all previous byte checksums (in one byte).

The host sends the bytes to the SPD1179 as follows:

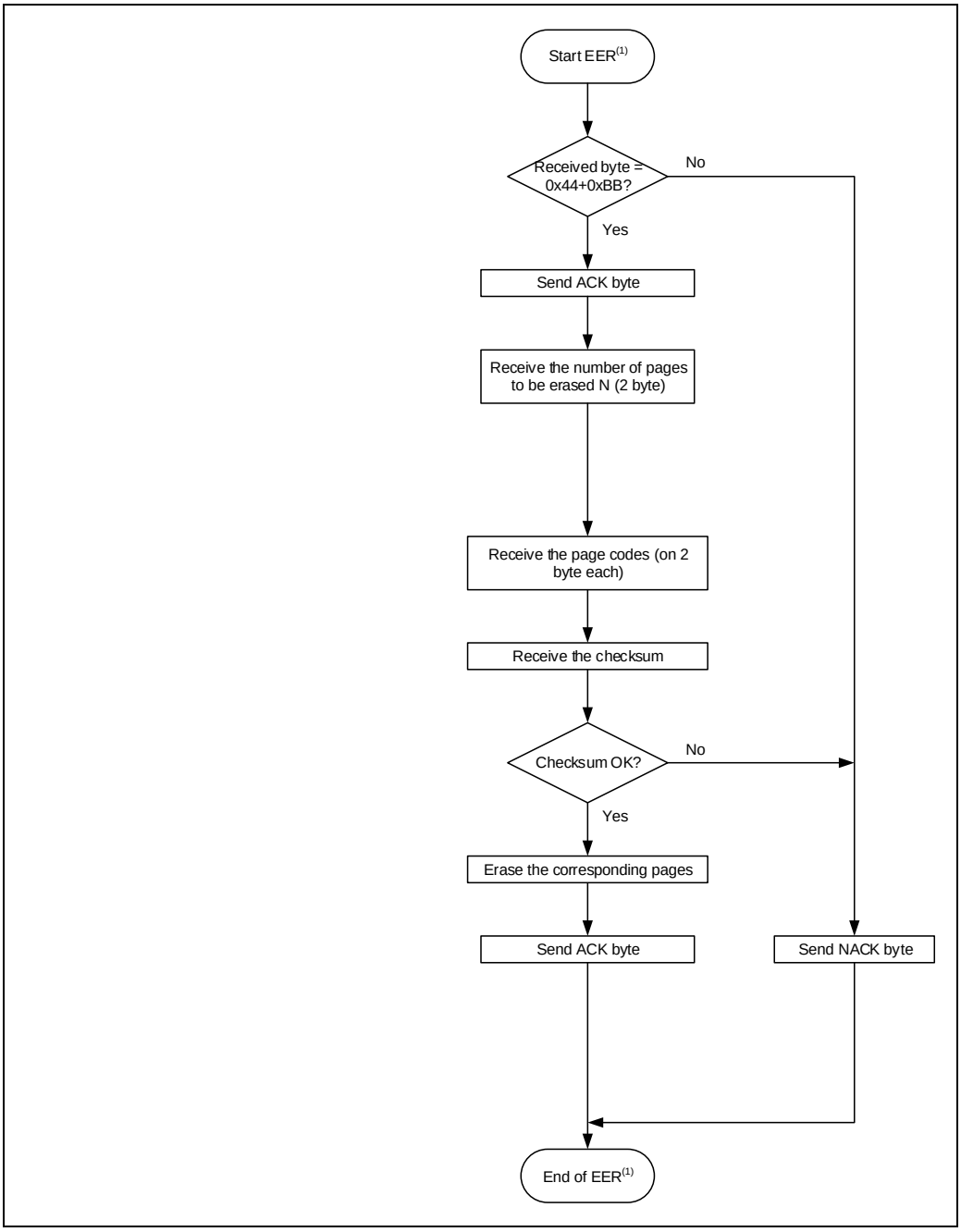
Byte 1:	0x44
Byte 2:	0xBB
	Wait for ACK
Bytes 3-4:	Number of pages to be erased (N+1 where: 0 ≤ N < Maximum number of pages).
Remaining bytes:	(2 x (N + 1)) bytes (page numbers coded on two bytes LSB first) and then the checksum for bytes 3-4 and all the following bytes)

Figure 6. Extended Erase Memory command: host side



1. EER = Extended Erase Memory.

Figure 7. Extended Erase Memory command: device side



1. EER = Extended Erase Memory.

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
12-Oct-2021	1	Initial release.